CHAPTER 4

MOS Field-Effect Transistors (MOSFETs)

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INTRODUCTION

- The basic principle involved is the use of the voltage between two terminals to control the current flowing in the third terminal.
- Also, in the extreme, the control signal can be used to cause the current in the third terminal to change from zero to a large value, thus allowing the device to act as a switch.
- There are two major types of three-terminal semiconductor device: the metal-oxide-semiconductor field-effect transistor (MOSFET), and bipolar junction transistor (BJT).

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- The MOSFET has become by far the most widely used electronic device, especially in the design of integrated circuits (ICs).
- Compared to BJTs, MOSFETs can be made quite small.Also, their operation requires comparatively little power.
- All of these properties have made it possible to pack large numbers of MOSFETs (>200 million!) on a single IC chip to implement very sophisticated, very-large-scale-integrated (VLSI) circuits.

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4.1 DEVICE STRUCTURE AND PHYSICAL OPERATION

4.1.1 Device Structure

- Figure 4.1 shows the physical structure of the n-channel enhancement-type MOSFET.
- The transistor is fabricated on a p-type substrate.
- Two heavily doped n-type regions, indicated in the figure as the n^+ **source** and the n^+ **drain** regions, are created in the substrate.

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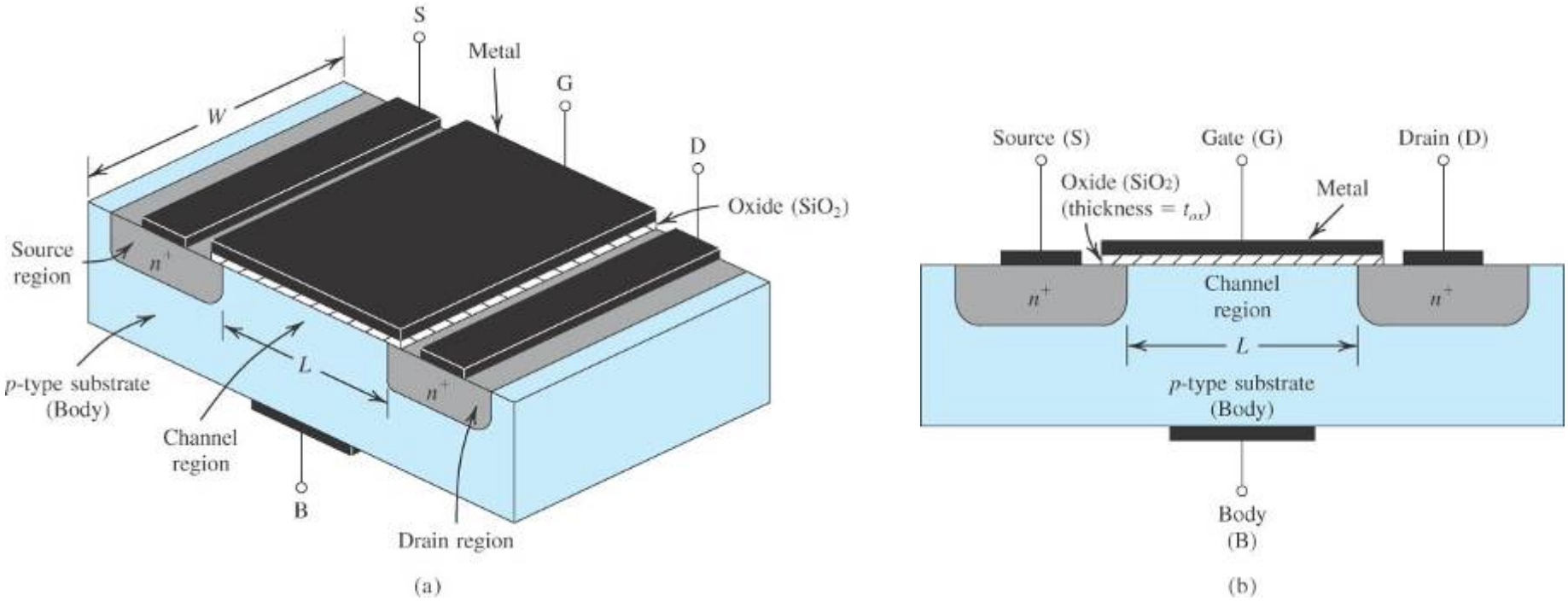

Figure 4.1 Physical structure of the enhancement-type NMOS transistor: **(a)** perspective view; **(b)** cross-section. Typically L = 0.1 to 3 μm, W = 0.2 to 100 μm, and the thickness of the oxide layer (t_{ox}) is in the range of 2 to 50 nm.

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- A thin layer of silicon dioxide (SiO_2) of thickness t_{ox} (typically 2-50 nm). which is an excellent electrical insulator, is grown on the surface of the substrate, covering the area between the source and drain regions.
- Metal is deposited on top of the oxide layer to form the **gate electrode.**
- Metal contacts are also made to the source region, the drain region, and the substrate, also known as the **body**.
- Thus four terminals are brought out: the gate terminal (G), the source terminal (S), the drain terminal (D), and the substrate or body terminal (B).

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- Another name for the MOSFET is the **insulated-gate FET** or **IGFET**.
- It will be shown that a voltage applied to the gate controls current flow between source and drain. This current will flow in the longitudinal direction from drain to source in the region labeled "channel region."
- Note that this region has a length L and a width W. Typically, L is in the range of 0.1 μm to 3 μm, and W is in the range of 0.2 μm to 100 μm.
- Finally, note that the MOSFET is a symmetrical device; thus its source and drain can be interchanged with no change in device characteristics.

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45奈米四核心CPU，Intel Penryn

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4.1.2 Operation with No Gate Voltage

- With no bias voltage applied to the gate, two back-to-back diodes exist in series between drain and source.
- These back-to-back diodes prevent current conduction from drain to source when a voltage v_{DS} is applied. In fact, the path between drain and source has a very high resistance (of the order of 10^{12} Ω).

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4.1.3 Creating a Channel for Current Flow

- In Fig. 4.2. Here we have grounded the source and the drain and applied a positive voltage to the gate.
- The positive voltage on the gate causes, in the first instance, the free holes (which are positive charged) to be repelled from the region of the substrate under the gate. These holes are pushed downward into the substrate, leaving behind a carrier-depletion region.

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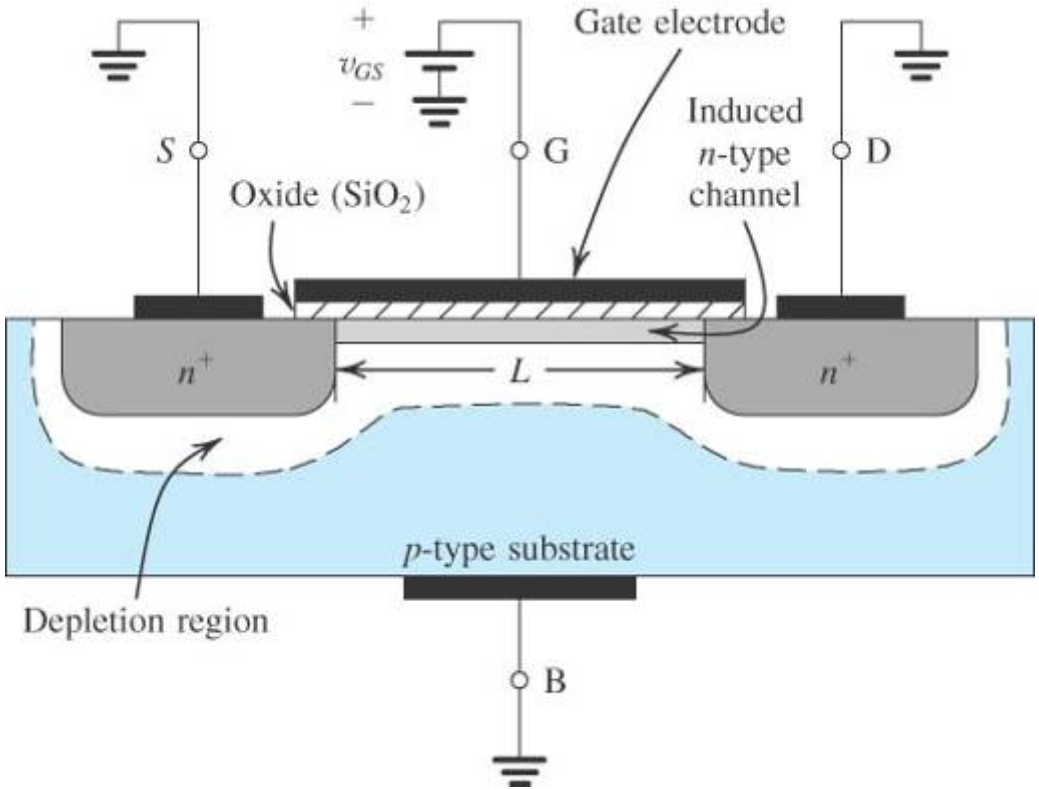

Figure 4.2 The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate.

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- As well, the positive gate voltage attracts electrons from the n^+ source and drain regions into the channel region.
- When a sufficient number of elections accumulate near the surface of the substrate under the gate, an n region is in effect created, connecting the source and drain regions, as indicated in Fig. 4.2.
- Now if a voltage is applied between drain and source, current flows through this induced n region.
- The induced *n* region thus forms a **channel** for current flow from drain to source.

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- The MOSFET of Fig. 4.2 is called an ***n*-channel MOSFET** or, alternatively, an **NMOS transistor**.
- The induced channel is also called an **inversion layer**.
- The value of v_{GS} at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the **threshold voltage** and is denoted V_t.
- The value of V_t is controlled during device fabrication and typically lies in the range of 0.5 V to 1.0V.

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- The gate and the channel region of the MOSFET form a parallel-plate capacitor, with the oxide layer acting as the capacitor dielectric.
- An electric field thus develops in the vertical direction. It is this field that controls the amount of charge in the channel, and thus it determines the channel conductivity and, in turn, the current that will flow through the channel when a voltage v_{DS} is appliled.

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4.1.4 Applying a Small V_{DS}

- We now apply a positive voltage v_{DS} between drain and source, as shown in Fig. 4.3.
- The voltage v_{DS} causes a current i_D to flow through the induced *n* channel. Current is carried by free electrons traveling from source to drain.
- The magnitude of i_D depends on the density of electrons in the channel, which in turn depends on the magnitude of v_{DS}.

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- Specifically, for $v_{GS} = V_t$, more electrons are attracted into the channel.
- The result is a channel of increased conductance or, equivalently, reduced resistance. In fact, the conductance of the channel is proportional to the **excess gate voltage** ($v_{GS} - V_t$), also known as the **effective voltage** or the **overdrive voltage**.
- Figure 4.4 shows a sketch of i_D versus v_{DS} for various values of v_{GS}. We observe that the MOSFET is operating as a linear resistance whose value is controlled by v_{GS}.

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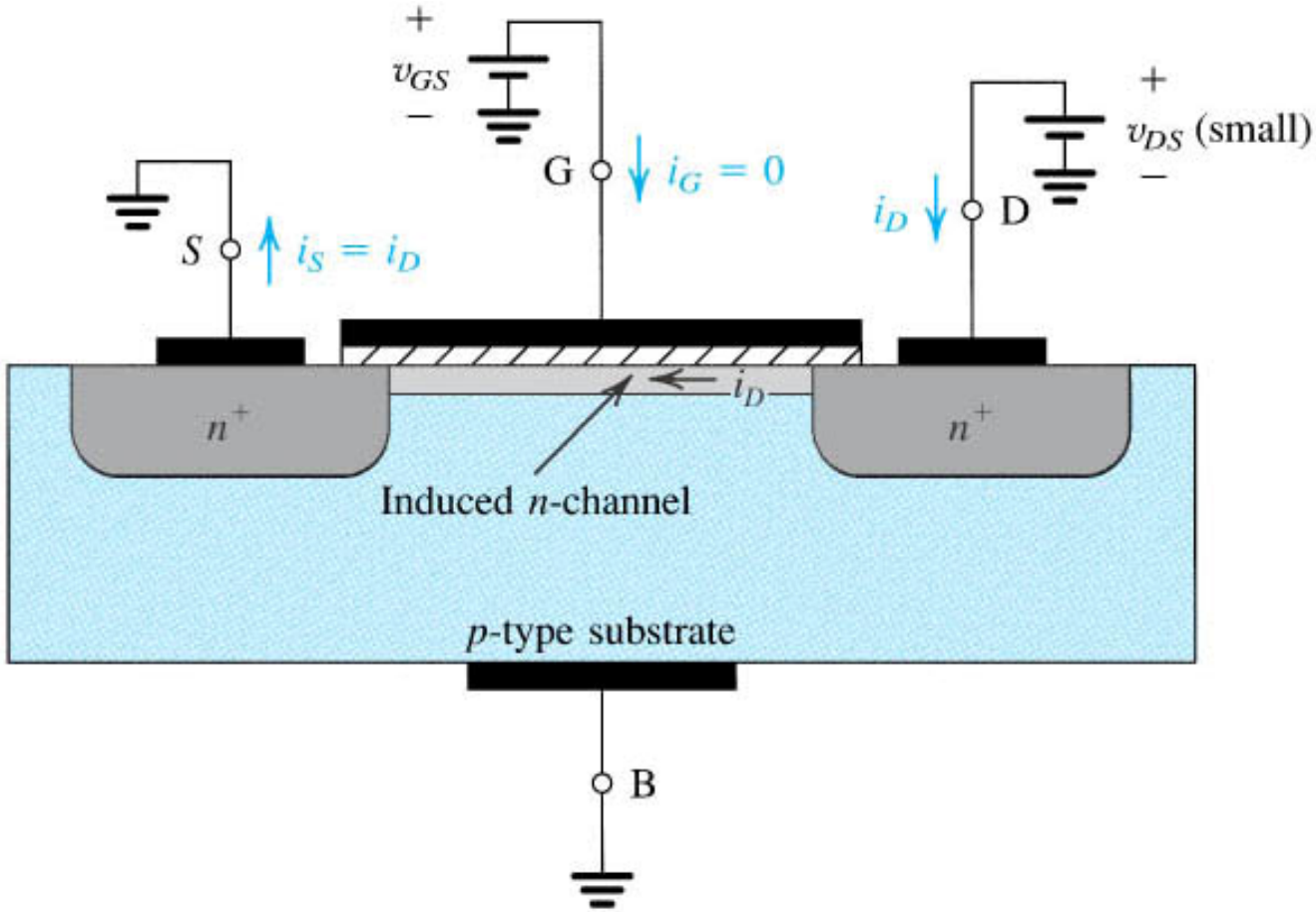

Figure 4.3 An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS}. Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and thus i_D is proportional to $(v_{GS} - V_t)\, v_{DS}$. Note that the depletion region is not shown (for simplicity).

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- The resistance is infinite for $v_{GS} \leqq V_t$, and its value decreases as v_{GS} exceeds V_t.
- Then, increasing v_{GS} above the threshold voltage V_t enhances the channel, hence names **enhancement-mode operation** and **enhancement-type MOSFET**.
- Finally, we note that the current that leaves the source terminal (i_S) is equal to the current that enters the drain terminal (i_D), and the gate current $i_G = 0$.

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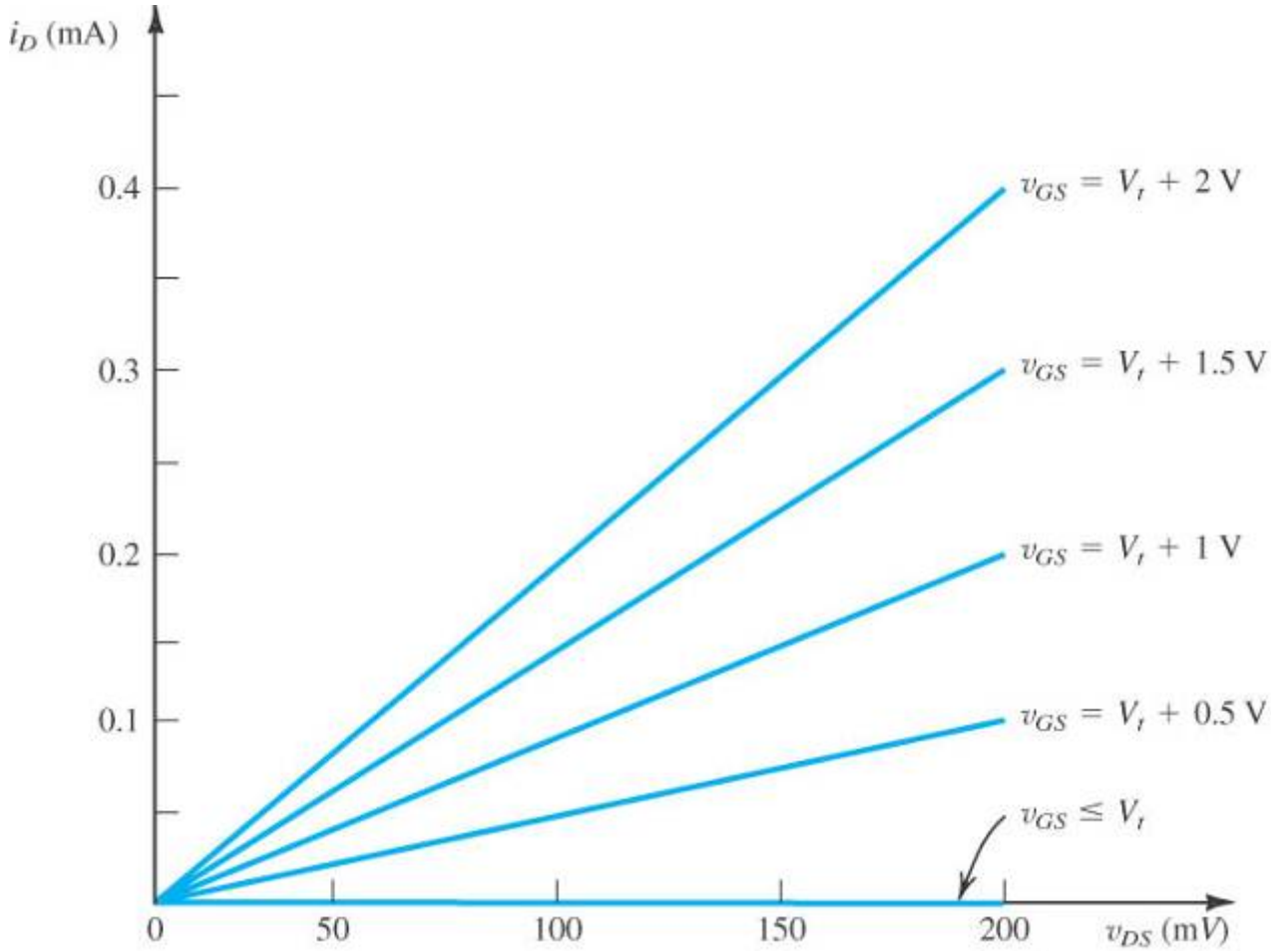

Figure 4.4 The i_D–v_{DS} characteristics of the MOSFET in Fig. 4.3 when the voltage applied between drain and source, $v_{DS,}$ is kept small. The device operates as a linear resistor whose value is controlled by v_{GS}.

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4.1.5 Operation as v_{DS} Is Increased

- As we travel along the channel from source to drain, the voltage (measured relative to the source) increases from 0 to v_{DS}.
- Thus the voltage between the gate and points along the channel decreases from v_{GS} at the source end to $v_{GS} - v_{DS}$ at the drain end.
- Since the channel depth depends on this voltage, we find that the channel is no longer of uniform depth.

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- As v_{DS} is increased, the channel becomes more tapered and its resistance increases correspondingly.
- When v_{DS} is increased to the value that reduces the voltage between gate and channel at the drain end to V_t ---that is,
- $v_{GD} = V_t$ or $v_{GS} - v_{DS} = V_t$ or $v_{DS} = v_{GS} - V_t$ the channel depth at the drain end decreases to almost zero, and the channel is said to be **pinched off**.

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- At the value reached for $v_{DS} = v_{GS} - V_t$. The drain current thus **saturates** at this value, and the MOSFET is said to have entered the saturation region of operation.

$$v_{DSsat} = v_{GS} - V_t \tag{4.1}$$

- The region of the $i_D - v_{DS}$ characteristic obtained for $v_{DS} < v_{DSsat}$ is called the **triode region**.

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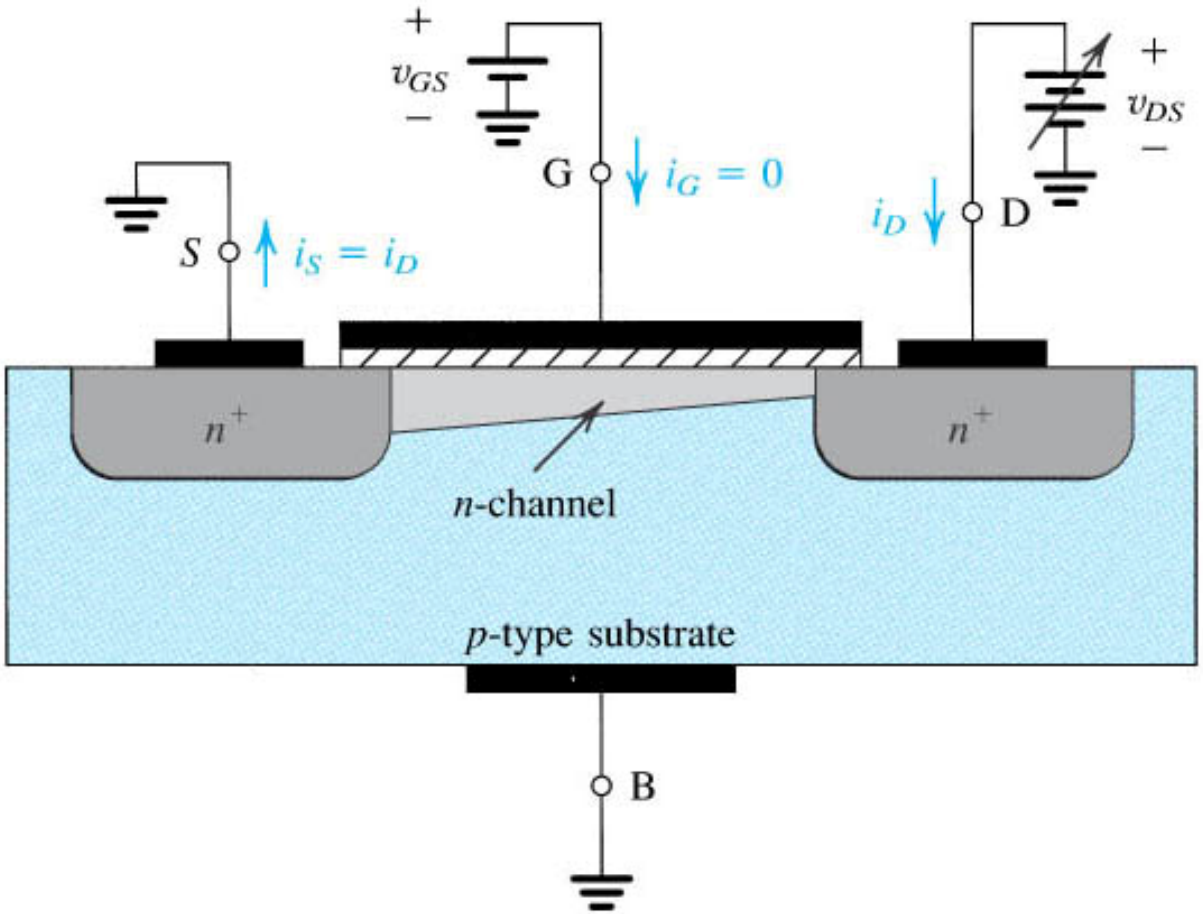

Figure 4.5 Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value > V_t.

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4.1.6 Derivation of the i_D-v_{DS} Relationship

- In the MOSFET, the gate and the channel region form a parallel-plate capacitor for which the oxide layer serves as a dielectric.
- If the capacitance per unit gate area is denoted C_{ox} and the thickness of the oxide layer is t_{ox}, then

$$C_{ox} = \varepsilon_{ox} / t_{ox} \qquad (4.2)$$

- Where ε_{ox} is the permittivity of the silicon oxide

$$\varepsilon = 3.9 \quad \varepsilon_0 = 3.9 \times 8.854 \times 10^{-12} = 3.45 \times 10^{-11} \text{ F/m}$$

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$$i_D = (\mu_n C_{ox})(\frac{W}{L})[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v^2{}_{DS}] \quad (4.5)$$

- The value of the current at the edge of the triode region or, equivalently, at the beginning of the saturation region can be obtained by substitutin $v_{DS} = v_{GS} - V_t$, resulting in

$$i_D = \frac{1}{2}(\mu_n C_{ox})(\frac{L}{W})(v_{GS} - V_t)^2 \quad (4.6)$$

- The **process transconductance parameter** is denoted k_n'

$$k_n' = \mu_n C_{ox} \quad (4.7)$$

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$$i_D = k_n' \frac{W}{L}[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v^2{}_{DS}] \quad \text{(triode region)} \qquad (4.5.a)$$

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_t)^2 \quad \text{(saturation region)} \qquad (4.6.a)$$

- The drain current is proportional to the ratio of the channel width W to the channel length L, known as the **aspect ratio** of the MOSFET.
- For a given fabrication process, however, there is a minimum channel length, L_{min}.

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- In fact, the minimum channel length that is possible with a given fabrication process is used to characterize the process and is being continually reduced as technology advances.
- MOS technology is a 0.13-μm process, meaning that for this process the minimum channel length possible is 0.13 μm.
- $t_{ox} = 2$nm.

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4.1.7 The p-Channel MOSFET

- A p-channel enhancement-type MOSFET (PMOS transistor), fabricated on an n-type with p^+ regions for the drain and source, has hoes as charge carriers.
- The device operates in the same manner as the n-channel device except that v_{GS} and v_{DS} are negative and the threshold voltage V_t is negative.
- Also, the current i_D enters the source terminal and leaves through the drain terminal.
- NMOS devices can be made smaller and thus operate faster, and because NMOS historically required lower supply voltages than PMOS.

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4.1.8 Complementary MOS or CMOS

- As the name implies, complementary MOS technology employs MOS transistors of both polarities.
- Indeed, at the present time CMOS is the most widely used of all the IC technologies.
- Figure 4.9 shows cross-section of a CMOS chip illustrating how the PMOS and NMOS transistors are fabricated. Observe that while the NMOS transistor is implemented directly in the p-type substrate, the PMOS transistor is fabricated in a specially created n region, known as an ***n* well**.

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4.2 CURRENT-VOLTAGE CHARACTERISTICS

4.2.1 Circuit Symbol

- *The drain is always positive relative to the source in an n-channel FET.*

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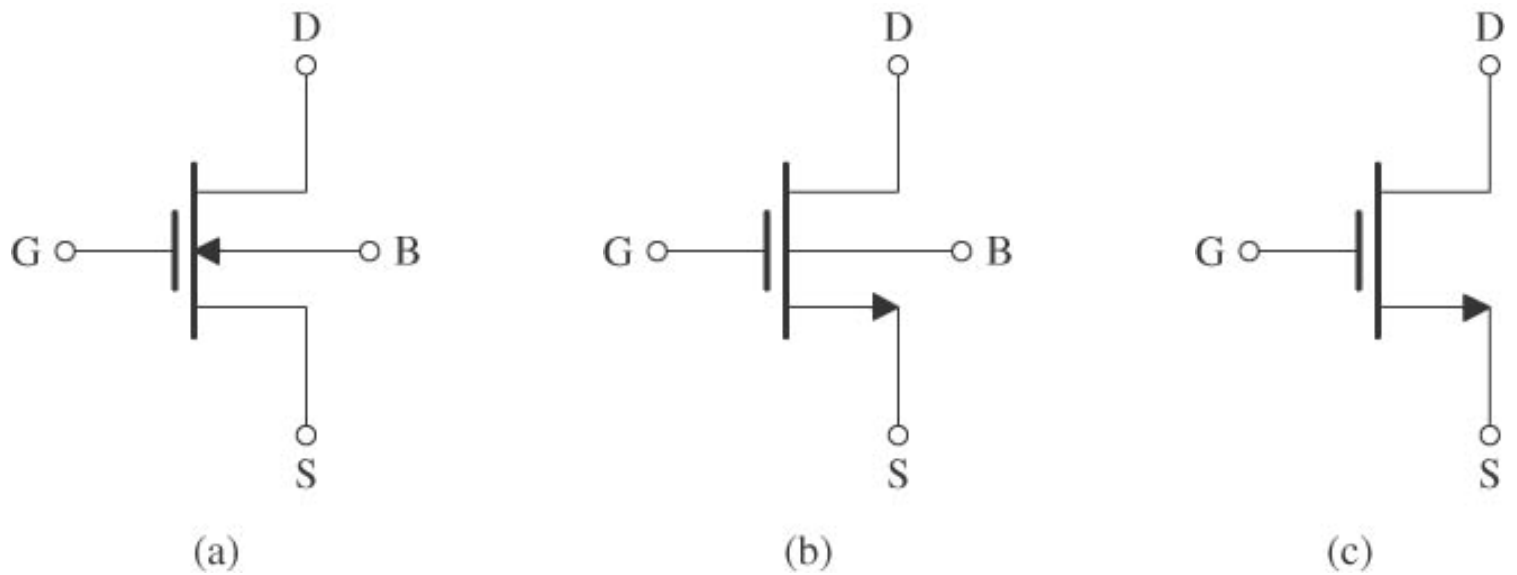

Figure 4.10 **(a)** Circuit symbol for the *n*-channel enhancement-type MOSFET. **(b)** Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e., *n* channel). **(c)** Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

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4.2.2 The i_D-v_{DS} Characteristics

- Figure 4.11(a) shows an n-channel enhancement-type MOSFET with voltages v_{GS} and v_{DS} applied and with the normal directions of current flow indicated.
- That there are three distinct regions of operation: the cutoff region, the **triode region**, and the **saturation region**.
- The saturation region is used if the FET is to operate as an amplifier.
- For operation as a switch, the cutoff and triode regions are utilized.

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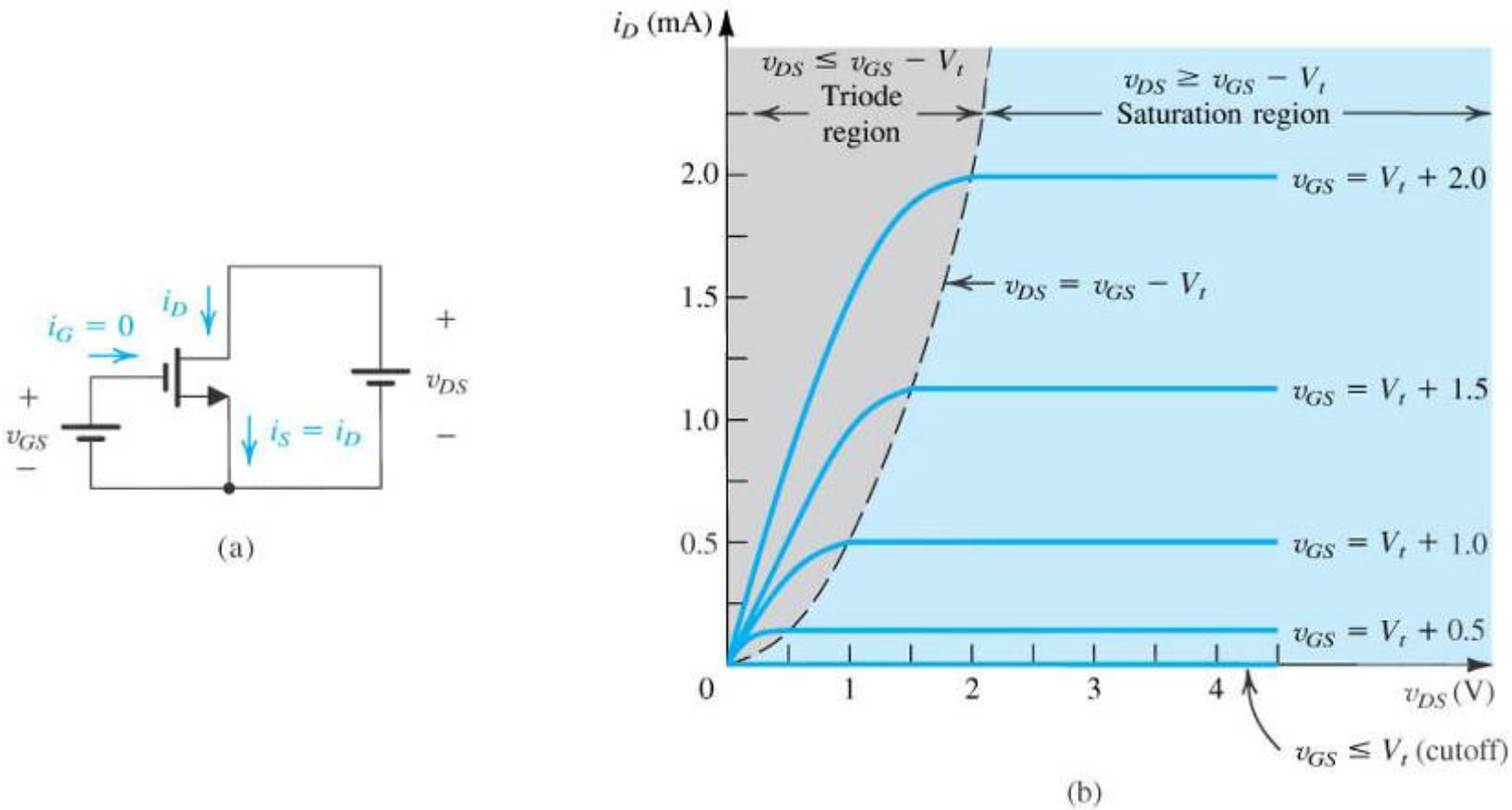

Figure 4.11 **(a)** An *n*-channel enhancement-type MOSFET with v_{GS} and v_{DS} applied and with the normal directions of current flow indicated. **(b)** The i_D–v_{DS} characteristics for a device with $k'_n(W/L) = 1.0$ mA/V^2.

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- To operate the MOSFET in the triode region we must first induce a channel,

  $v_{GS} \geqq V_t$ (Induced channel) (4.8)

- And then keep v_{DS} small enough so that the channel remains continuous. This is achieved by ensuring that the gate-to-drain voltage is

  $v_{GD} \geqq V_t$ (Continuous channel) (4.9)

  $v_{GD} = v_{GS} + v_{SD} = v_{GS} - v_{DS}$;

  $v_{GS} - v_{DS} > V_t$

  $v_{DS} < v_{GS} - V_t$ (Continuous channel) (4.10)

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- *The n-channel enhancement-type MOSFET operates in the triode region when v_{GS} is greater than V_t and the drain voltage is lower than the gate voltage by at least V_t volts.*
- In the triode region, the i_D-v_{DS} characteristics can be described by

$$i_D = k_n' \frac{W}{L}[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v^2{}_{DS}] \qquad (4.11)$$

where $k_n' = \mu_n C_{ox}$ is the process transconductance parameter.

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- If v_{DS} is sufficiently small

$$i_D \cong k_n' \frac{W}{L}(v_{GS} - V_t)v_{DS} \tag{4.12}$$

- Specifically, for v_{GS} set to a value V_{GS}, r_{DS} is given by

$$r_{DS} \equiv \frac{v_{DS}}{i_D}\bigg|_{\substack{v_{DSsmall} \\ v_{GS}=V_{GS}}} = [k_n' \frac{W}{L}(v_{GS} - V_t)]^{-1} \tag{4.13}$$

- It is also useful to express r_{DS} in terms of the **gate-to-source overdrive voltage**

$$V_{OV} = V_{GS} - V_t \tag{4.14}$$

$$r_{DS} = 1/[k_n'(\frac{W}{L})V_{OV}] \tag{4.15}$$

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- To operate the MOSFET I the saturation region, a channel must be induced,

$$v_{GS} \geqq V_t \quad \text{(Induced channel)} \qquad (4.16)$$

$$v_{GD} \leqq V_t \quad \text{(Pinched-off channel)} \qquad (4.17)$$

$$v_{DS} \geqq v_{GS} - V_t \quad \text{(Pinched-off channel)} \qquad (4.18)$$

- *The n-channel enhancement-type MOSFET operates in the saturation region when v_{GS} is greater than V_t and the drain voltage does not fall below the gate voltage by more than V_t volts.*
- The boundary between the triode region and the saturation region is characterized by

$$v_{DS} = v_{GS} - V_t \quad \text{(Boundary)} \qquad (4.19)$$

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- Substituting this value of V_{DS} into Eq. (4.11)

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2 \qquad (4.20)$$

- Since the drain current is independent of the drain voltage, the saturate MOSFET behaves as an ideal current source whose value is controlled by v_{GS} according to the nonlinear relationship in Eq. (4.20).
- Figure 4.13 shows a circuit representation of this view of MOSFET operation in the saturation region. Note that this is a **large-signal equivalent-circuit model.**

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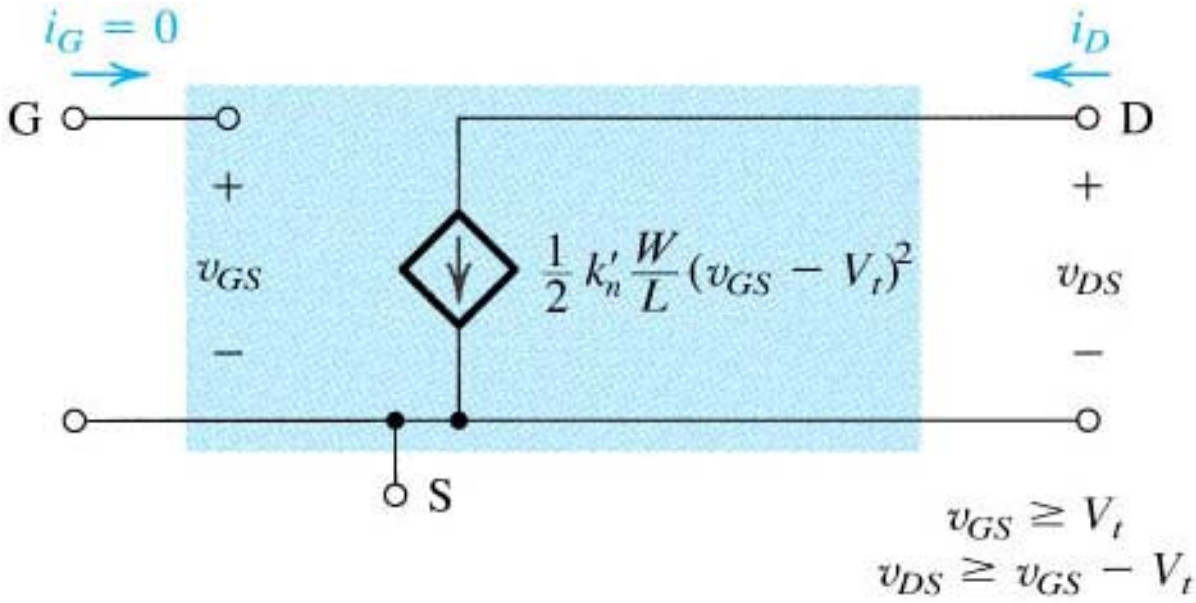

Figure 4.13 Large-signal equivalent-circuit model of an *n*-channel MOSFET operating in the saturation region.

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4.2.4 Characteristics of the *p*-Channel MOSFET

- The circuit symbol for the p-channel enhancement-type MOSFET is shown in Fig. 4.18(a).
- Recall that for the p-channel device the threshold voltage V_t is negative. To induce a channel we apply a gate voltage that is more negative than V_t.

$$v_{GS} \leqq V_t \tag{4.27}$$

- And apply a drain voltage that is more negative than the source voltage.

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- To operate in the triode region V_{DS} must satisfy

$$v_{DS} \geqq v_{GS} - V_t \tag{4.28}$$

- This is, the drain voltage must be higher than the gate voltage by at least $|V_t|$.

$$i_D = k_p' \frac{W}{L}[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v^2{}_{DS}] \tag{4.29}$$

$$k_p' = \mu_p C_{ox} \tag{4.30}$$

- Operate in saturation, v_{DS} must satisfy the relationship

$$v_{DS} \leqq v_{GS} - V_t \tag{4.31}$$

$$i_D = \frac{1}{2} k_p' \frac{W}{L}(v_{GS} - V_t)^2(1 + \lambda v_{DS}) \tag{4.32}$$

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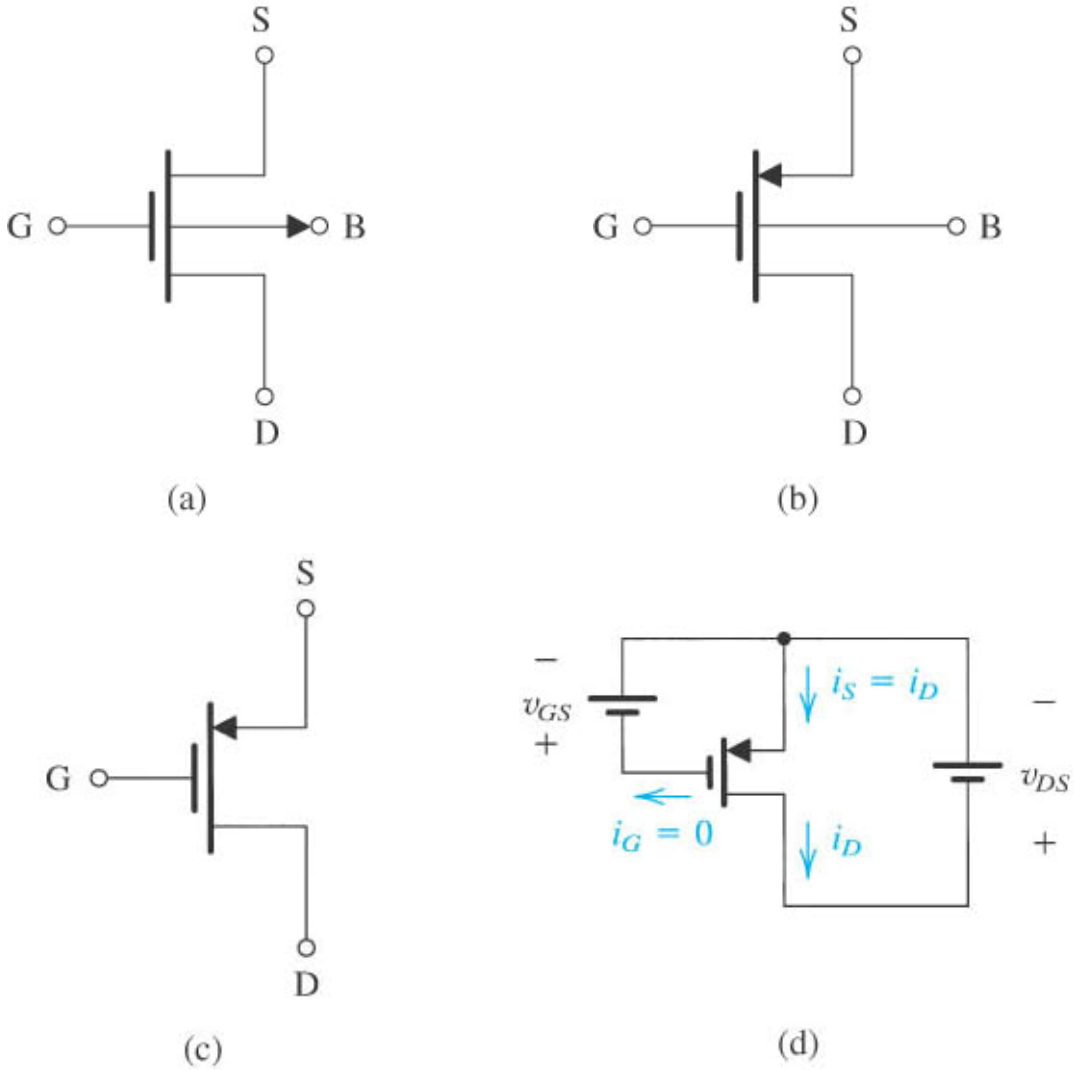

Figure 4.18 **(a)** Circuit symbol for the *p*-channel enhancement-type MOSFET. **(b)** Modified symbol with an arrowhead on the source lead. **(c)** Simplified circuit symbol for the case where the source is connected to the body. **(d)** The MOSFET with voltages applied and the directions of current flow indicated. Note that v_{GS} and v_{DS} are negative and i_D flows out of the drain terminal.

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4.2.5 The Role of the Substrate--- The body Effect

- The body voltage control i_D; thus the body acts as another gate for the MOSFET, a phenomenon known as the **body effect**.
- Here we note that the parameter γ is known as the **body-effect parameter**.

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4.2.6 Temperature Effects

- The magnitude of V_t decreases by about 2 mV for every 1^{o}C rise in temperature.
- This decrease in $|V_t|$ gives rise to a corresponding increase in drain current as temperature is increased.

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4.3 MOSFET CIRCUITS AT DC

EXAMPLE 4.2

Design the circuit of Fig. 4.20 so that the transistor operates at $I_D = 0.4$ mA and $V_D = +0.5$ V. The NMOS transistor has $V_t = 0.7$ V, $\mu_n C_{ox} = 100\ \mu\text{A/V}^2$, $L = 1\ \mu$m, and $W = 32\ \mu$m. Neglect the channel-length modulation effect (i.e., assume that $\lambda = 0$).

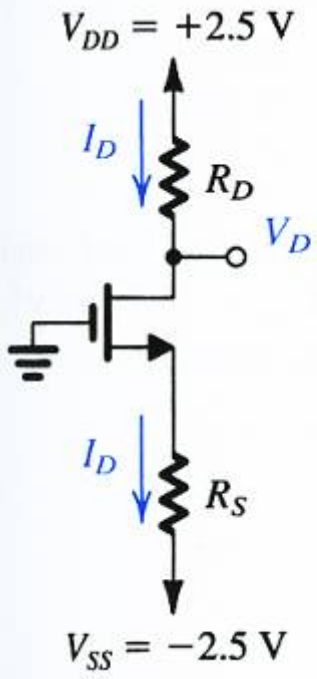

FIGURE 4.20 Circuit for Example 4.2.

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Solution

Since $V_D = 0.5$ V is greater than V_G, this means the NMOS transistor is operating in the saturation region, and we use the saturation-region expression of i_D to determine the required value of V_{GS},

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

Substituting $V_{GS} - V_t = V_{OV}$, $I_D = 0.4$ mA $= 400\ \mu$A, $\mu_n C_{ox} = 100\ \mu$A/V^2, and $W/L = 32/1$ gives

$$400 = \frac{1}{2} \times 100 \times \frac{32}{1} V_{OV}^2$$

which results in

$$V_{OV} = 0.5 \text{ V}$$

Thus,

$$V_{GS} = V_t + V_{OV} = 0.7 + 0.5 = 1.2 \text{ V}$$

Referring to Fig. 4.20, we note that the gate is at ground potential. Thus the source must be at -1.2 V, and the required value of R_S can be determined from

$$R_S = \frac{V_S - V_{SS}}{I_D} = \frac{-1.2 - (-2.5)}{0.4} = 3.25 \text{ k}\Omega$$

To establish a dc voltage of +0.5 V at the drain, we must select R_D as follows:

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{2.5 - 0.5}{0.4} = 5 \text{ k}\Omega$$

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EXAMPLE 4.5

Analyze the circuit shown in Fig. 4.23(a) to determine the voltages at all nodes and the currents through all branches. Let $V_t = 1$ V and $k_n'(W/L) = 1$ mA/V^2. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).

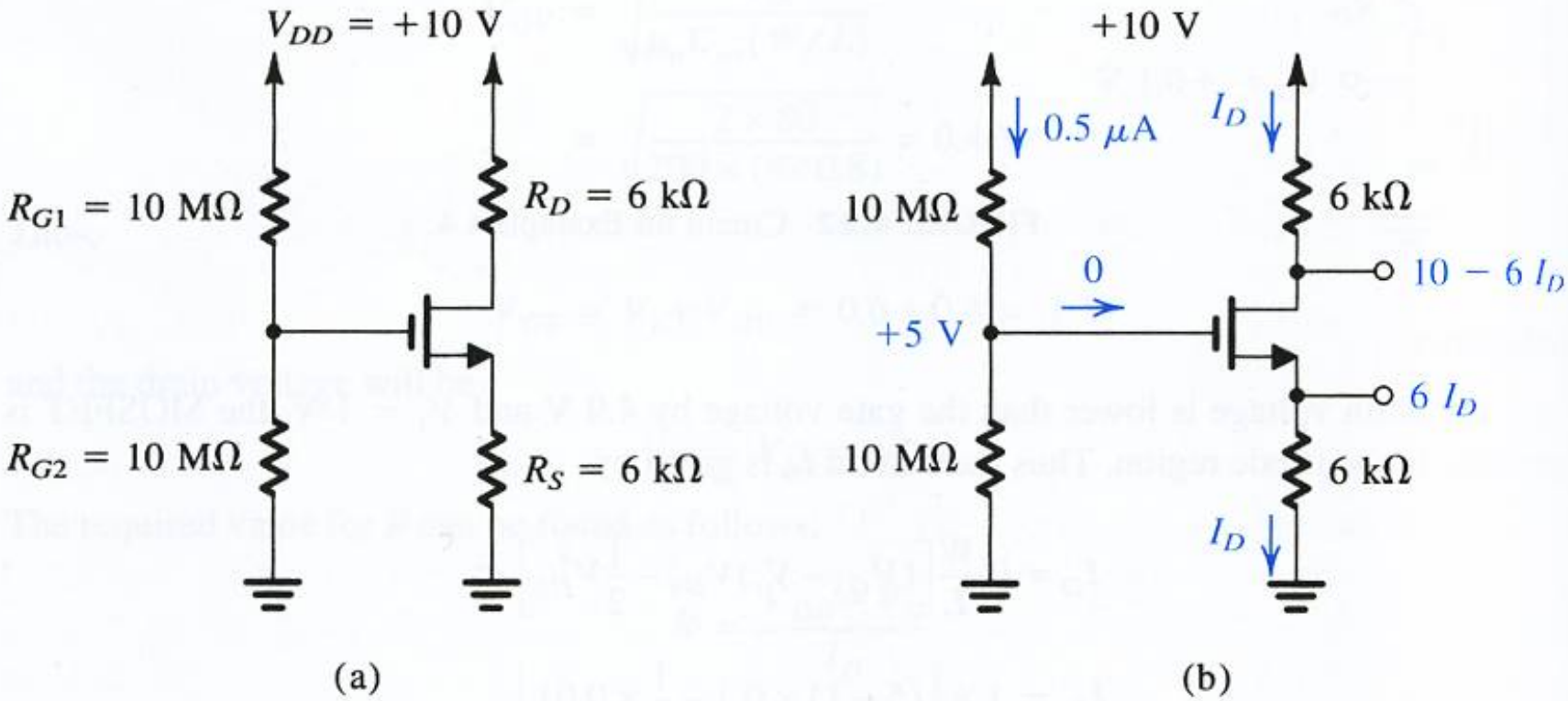

FIGURE 4.23 **(a)** Circuit for Example 4.5. **(b)** The circuit with some of the analysis details shown.

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Solution

Since the gate current is zero, the voltage at the gate is simply determined by the voltage divider formed by the two 10-MΩ resistors,

$$V_G = V_{DD}\frac{R_{G2}}{R_{G2}+R_{G1}} = 10\times\frac{10}{10+10} = +5\text{ V}$$

With this positive voltage at the gate, the NMOS transistor will be turned on. We do not know, however, whether the transistor will be operating in the saturation region or in the triode region. We shall assume saturation-region operation, solve the problem, and then check the validity of our assumption. Obviously, if our assumption turns out not to be valid, we will have to solve the problem again for triode-region operation.

Refer to Fig. 4.23(b). Since the voltage at the gate is 5 V and the voltage at the source is I_D (mA) × 6 (kΩ) = $6I_D$ (V), we have

$$V_{GS} = 5 - 6I_D$$

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Thus I_D is given by

$$I_D = \frac{1}{2}k_n' \frac{W}{L}(V_{GS} - V_t)^2$$

$$= \frac{1}{2} \times 1 \times (5 - 6I_D - 1)^2$$

which results in the following quadratic equation in I_D:

$$18I_D^2 - 25I_D + 8 = 0$$

This equation yields two values for I_D: 0.89 mA and 0.5 mA. The first value results in a source voltage of $6 \times 0.89 = 5.34$, which is greater than the gate voltage and does not make physical sense as it would imply that the NMOS transistor is cut off. Thus,

$$I_D = 0.5 \text{ mA}$$
$$V_S = 0.5 \times 6 = +3 \text{ V}$$
$$V_{GS} = 5 - 3 = 2 \text{ V}$$
$$V_D = 10 - 6 \times 0.5 = +7 \text{ V}$$

Since $V_D > V_G - V_t$, the transistor is operating in saturation, as initially assumed.

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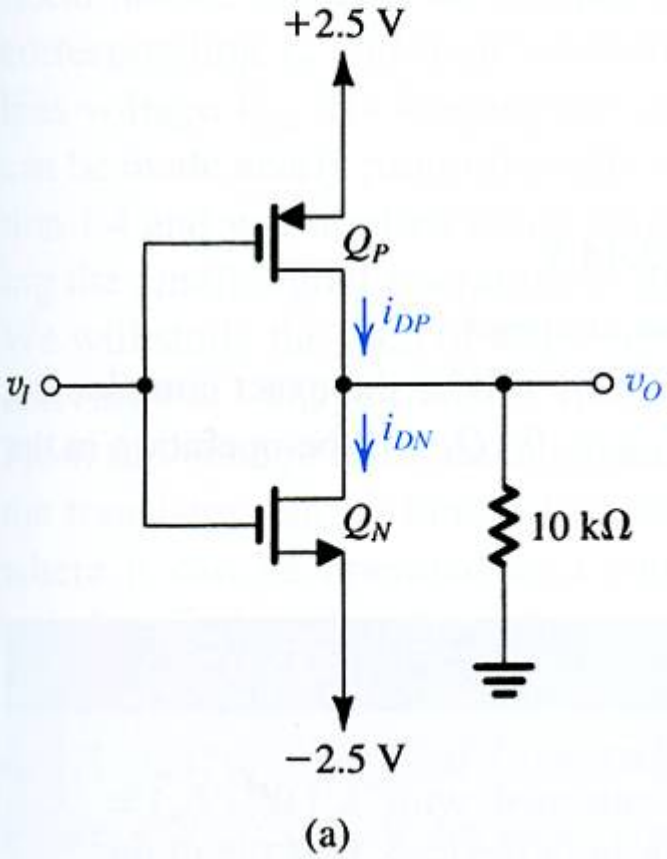
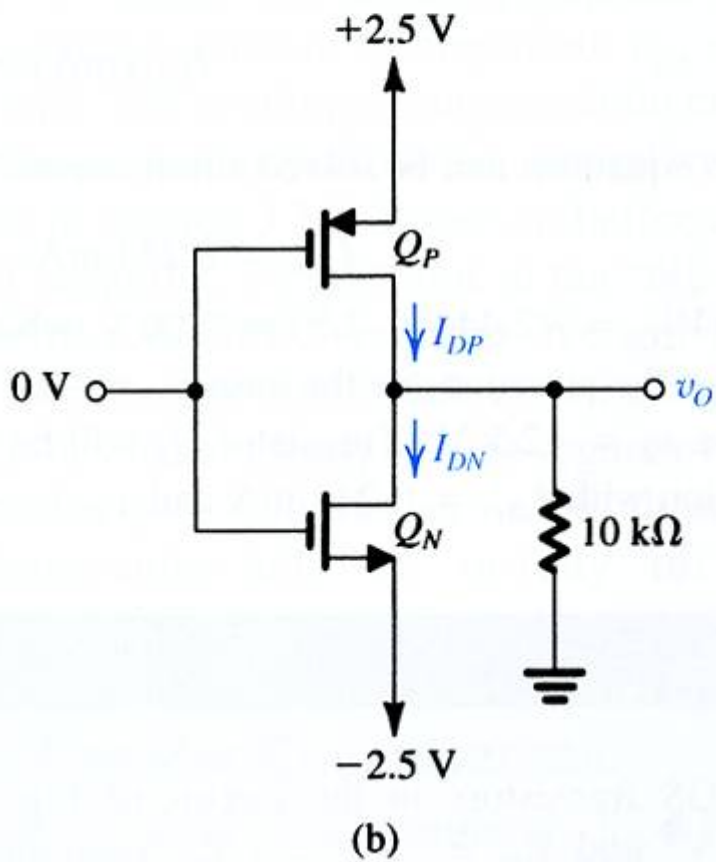
EXAMPLE 4.7

The NMOS and PMOS transistors in the circuit of Fig. 4.25(a) are matched with $k_n'(W_n/L_n) = k_p'(W_p/L_p) = 1\ \text{mA/V}^2$ and $V_{tn} = -V_{tp} = 1\ \text{V}$. Assuming $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP}, as well as the voltage v_O, for $v_I = 0\ \text{V}$, +2.5 V, and −2.5 V.



(a)



(b)

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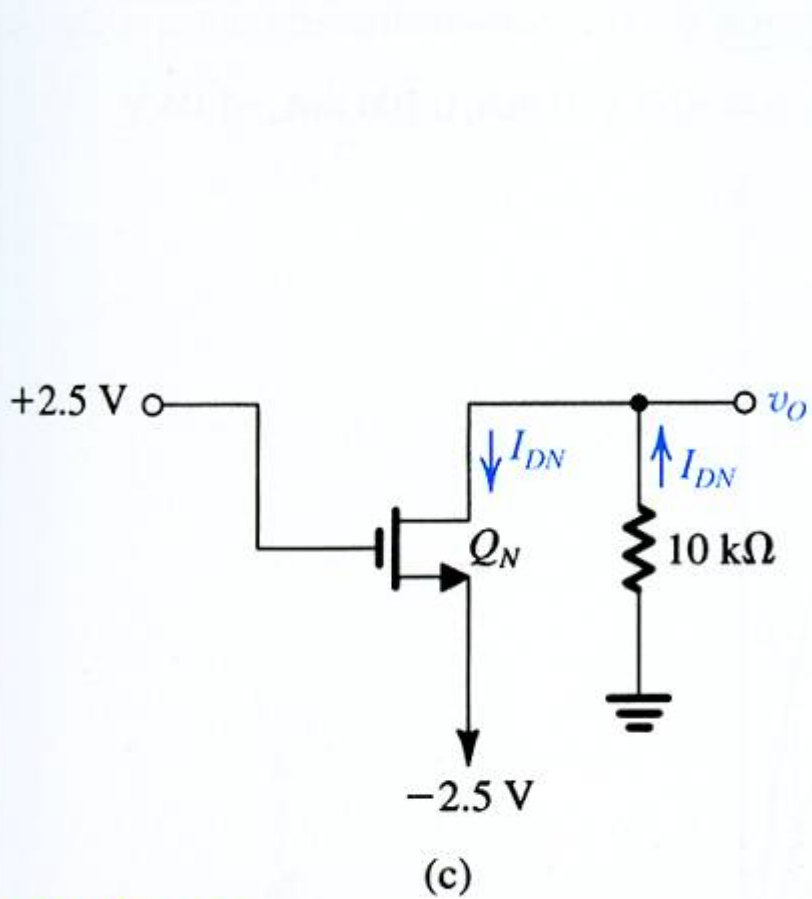

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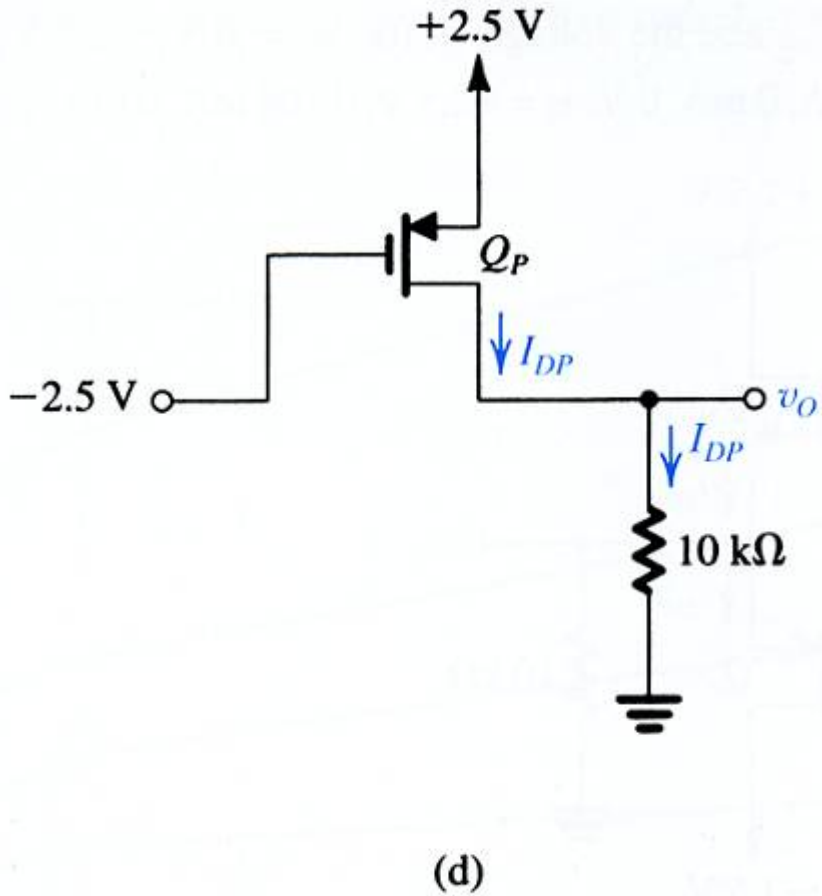

(d)

FIGURE 4.25 Circuits for Example 4.7.

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Solution

Figure 4.25(b) shows the circuit for the case $v_I = 0$ V. We note that since Q_N and Q_P are perfectly matched and are operating at equal $|V_{GS}|$ (2.5 V), the circuit is symmetrical, which dictates that $v_O = 0$ V. Thus both Q_N and Q_P are operating with $|V_{DG}| = 0$ and, hence, in saturation. The drain currents can now be found from

$$I_{DP} = I_{DN} = \tfrac{1}{2} \times 1 \times (2.5 - 1)^2$$
$$= 1.125 \text{ mA}$$

Next, we consider the circuit with $v_I = +2.5$ V. Transistor Q_P will have a V_{GS} of zero and thus will be cut off, reducing the circuit to that shown in Fig. 4.25(c). We note that v_O will be negative, and thus v_{GD} will be greater than V_t, causing Q_N to operate in the triode region. For simplicity we shall assume that v_{DS} is small and thus use

$$I_{DN} \cong k_n'(W_n/L_n)(V_{GS} - V_t)V_{DS}$$
$$= 1[2.5 - (-2.5) - 1][v_O - (-2.5)]$$

From the circuit diagram shown in Fig. 4.25(c), we can also write

$$I_{DN}\,(\text{mA}) = \frac{0 - v_O}{10\,(\text{k}\Omega)}$$

These two equations can be solved simultaneously to yield

$$I_{DN} = 0.244 \text{ mA} \qquad v_O = -2.44 \text{ V}$$

Note that $V_{DS} = -2.44 - (-2.5) = 0.06$ V, which is small as assumed.

Finally, the situation for the case $v_I = -2.5$ V [Fig. 4.25(d)] will be the exact complement of the case $v_I = +2.5$ V: Transistor Q_N will be off. Thus $I_{DN} = 0$, Q_P will be operating in the triode region with $I_{DP} = 0.244$ mA and $v_O = +2.44$ V.

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4.4 THE MOSFET AS AN AMPLIFIER AND AS A SWITCH

4.4.1 Large-Signal Operation-The Transfer Characteristic

- Figure 4.26(a) shows the basic structure (skeleton) of the most commonly used MOSFET amplifier, the **common-source (CS)** circuit or **ground-source.**

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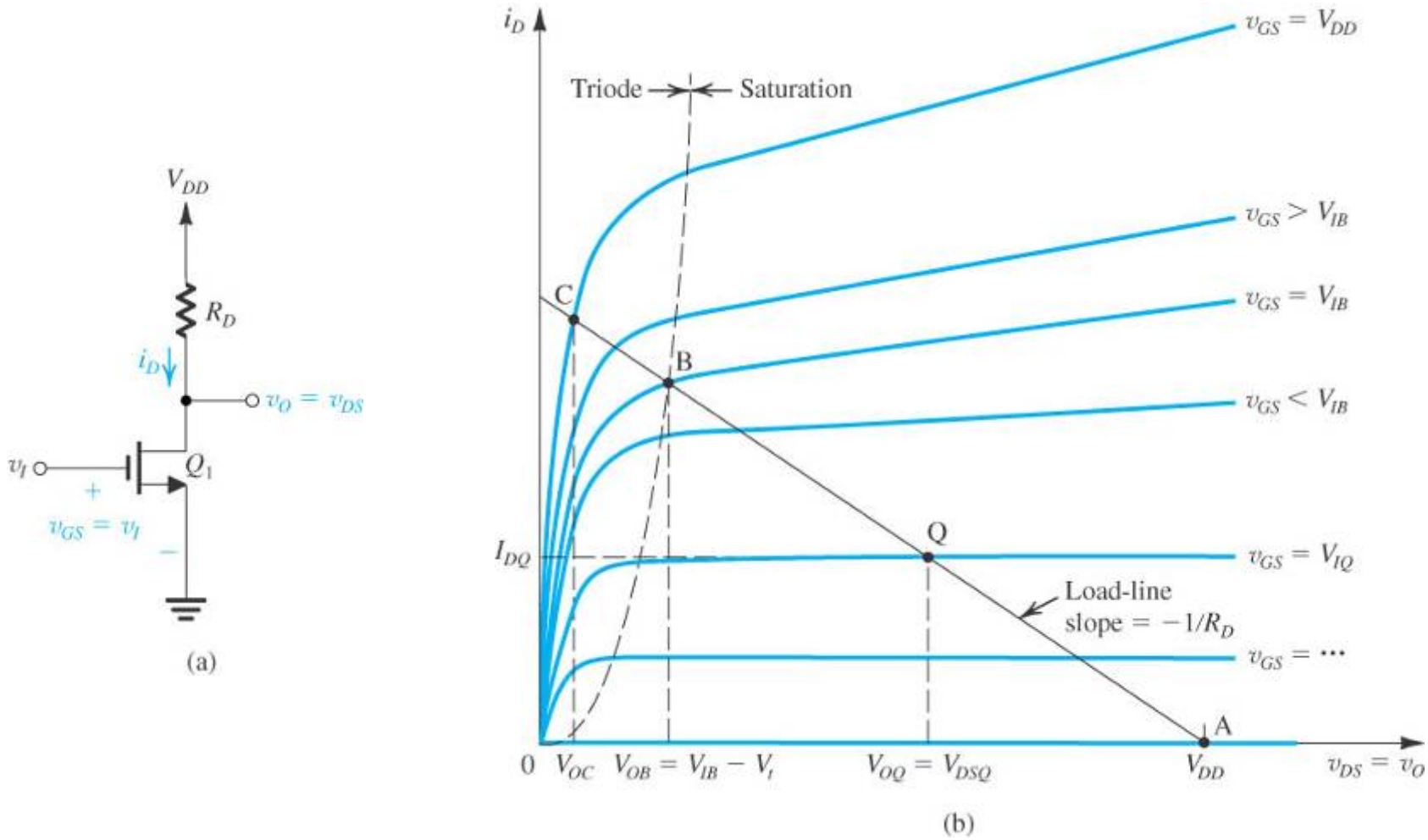

Figure 4.26 (a) Basic structure of the common-source amplifier. **(b)** Graphical construction to determine the transfer characteristic of the amplifier in (a).

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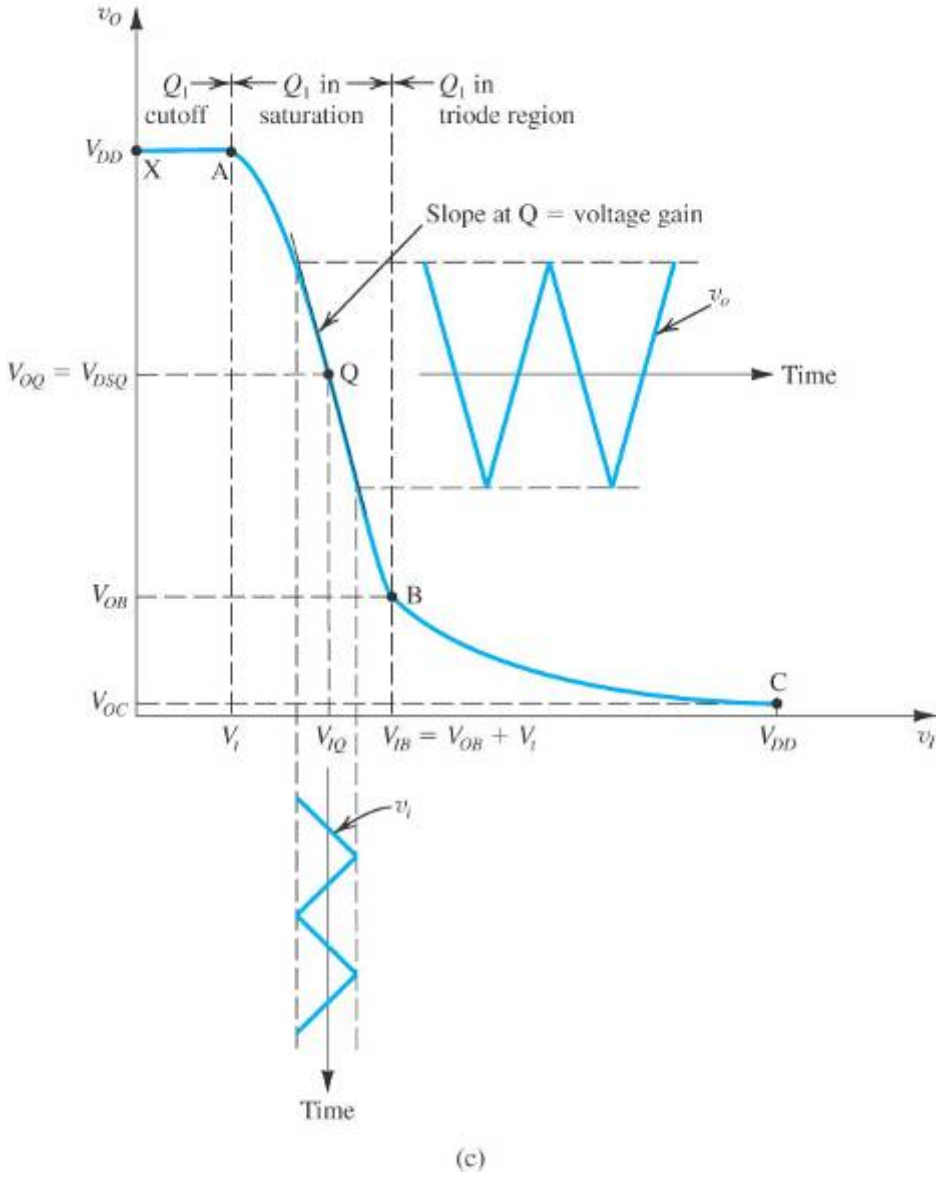

Figure 4.26 *(Continued)* **(c)** Transfer characteristic showing operation as an amplifier biased at point Q.

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- The basic control action of the MOSFET is that changes in v_{GS} (here, changes in v_I as $v_{GS}=v_I$) give rise to changes in i_D, we are using a resistor R_D to obtain an output voltage v_o

$$v_O=v_{DS}=V_{DD}-R_D i_D \tag{4.35}$$

$$i_D = \frac{V_{DD}}{R_D} - \frac{1}{R_D} v_{DS} \tag{4.37}$$

- Figure 4.26(b) shows a sketch of MOSFET's i_D-v_{DS} characteristic curves superimposed on which is a straight line representing the i_D-v_{DS} relationship of Eq.(4.37). The straight line in Fig.4.26(b) is known as the **load line**.

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- For any given value of $v_I < V_t$, the transistor will be cut off, i_D-v_{DS} curve and find v_o from the point of intersection of this curve with the load line.
- The circuit works as follows: Since $v_{GS}=v_I$, we see that for $v_I < V_t$, the transistor will be cut off, i_D will be zero, and $v_o=v_{GS}=V_{DD}$. Operation will be at the point labeled A.
- As v_I exceeds V_t, the transistor turns on, i_D increases, and v_o decreases. Since v_o will initially be high, the transistor will be operating in the saturation region.
- This corresponds to points along the segment of the load line from A to B.

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- It is obtained for $V_{GS}=V_{IQ}$ and has the coordinates $V_{OQ}=V_{DSQ}$ and I_{DQ}.
- Saturation-region operation continues until V_o decreases to the point that it is below vi by V_t volts.
- At this point . $v_{DS}=v_{GS}-V_t$, and the MOSEFT enters its triode region of operation.This is indicate in Fig.4.26(b) by point B.
- Point B is defined by $V_{OB}=V_{IB}-V_t$
- For $V_I > V_{IB}$, the transistor is driven deeper into the triode region. The output voltage decreases slowly towards zero.
- Point C obtained for $v_I = V_{DD}$.

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4.4.3 Operation as a Switch

- When the MOSFET is used as a switch, it is operated at the extreme points of the transfer curve.
- Specifically, the device is turned off by keeping $v_I < V_t$ resulting in operation somewhere on the segment **XA** with $v_o = V_{DD}$.
- The switch is turned on by applying a voltage close to V_{DD}, resulting in operation close to point C with v_o very small (at C, $v_o = V_{oc}$).
- The common-source MOS circuit can be used as a logic inverter with the "low" voltage level close to 0 V and the "high" level close to V_{DD}.
- More elaborate MOS logic inverters are studied in Section 4.10.

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4.4.4 Operation as a Linear Amplifier

- To operate the MOSFET as an amplifier we make use of the saturation-mode segment of the transfer curve.
- The device is biased at a point located somewhere close to the middle of the curve; point Q called the **quiescent point**.
- The voltage signal to be amplified v_i is then superimposed on the dc voltage V_{IQ} as shown in Fig.4.26(c).

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- That is, the amplifier will be very linear, and v_o will have the same waveform as v_i except that it will be larger by a factor equal to the voltage gain of the amplifier at Q:

$$A_v \equiv \left.\frac{dv_O}{dv_I}\right|_{v_I = V_{IQ}}$$

- The voltage gain is equal to the slope of the transfer curve at the bias point Q.
- Observe that the slope is negative, and thus the basic CS amplifier is inverting.

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4.4.5 Analytical Expressions for the Transfer Characteristic

- The Cutoff-Region Segment, XA

  Here, $v_I \leqq V_t$, and $v_o \geqq V_{DD}$.

- The Saturation-Region Segment, AQB

  $v_I \geqq V_t$, and $v_o \geqq v_I - V_t$.

$$v_O = V_{DD} - \frac{1}{2} R_D \mu_n C_{OX} \frac{W}{L} (v_I - V_t)^2 \tag{4.39}$$

$$A_v \equiv \left. \frac{dv_O}{dv_I} \right|_{v_I = V_{IQ}}$$

$$A_v = -R_D \mu_n C_{OX} \frac{W}{L} (V_{IQ} - V_t) \tag{4.40}$$

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- Another simple and very useful expression for the voltage gain can be obtained by substituting $v_I = V_{IQ}$ and $v_o = V_{OQ}$ in Eq. (4.39), utilizing Eq. (4.40), and substituting $V_{IQ} - V_t = V_{OV}$. The result is

$$A_v = -\frac{2(V_{DD} - V_{OQ})}{V_{OV}} = -\frac{2V_{RD}}{V_{OV}} \qquad (4.41)$$

  where V_{RD} is the dc voltage across the drain resistor R_D; that is, $V_{RD} = V_{DD} - V_{OQ}$.

- The end point of the saturation-region segment is characterized by

$$V_{OB} = V_{IB} - V_t \qquad (4.42)$$

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- The Triode-Region Segment, BC

  Here, $v_I \geqq V_t$, and $v_o \leqq v_I$-V_t.

$$v_O = V_{DD} - R_D \mu_n C_{OX} \frac{W}{L}[(v_I - V_t)v_O - \frac{1}{2}v_O^2]$$

$$v_O \cong V_{DD} - R_D \mu_n C_{OX} \frac{W}{L}(v_I - V_t)v_O \qquad (4.43)$$

$$v_O = V_{DD} / [1 + R_D \mu_n C_{OX} \frac{W}{L}(v_I - V_t)]$$

$$r_{DS} = 1/[\mu_n C_{OX} \frac{W}{L}(v_I - V_t)]$$

$$v_O = V_{DD} \frac{r_{DS}}{r_{DS} + R_D} \qquad (4.44)$$

Usually, $r_{DS} << R_D$

$$v_O \cong V_{DD} \frac{r_{DS}}{R_D} \qquad (4.45)$$

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4.5 BIASING IN MOS AMPLIFIER CIRCUITS

- An essential step in the design of a MOSFET amplifier circuit is the establishment of an appropriate dc operating point for the transistor.
- This is the step known as biasing or bias design.

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4.5.1 Biasing by Fixing V_{GS}

- The most straightforward approach to biasing a MOSFET is to fix its gate-to-source voltage V_{GS} to the value required to provide the desired I_D.

$$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{GS} - V_t)^2$$

- Biasing by fixing V_{GS} is not a good technique.

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4.5.2 Biasing by Fixing V_G and Connecting a Resistance in the Source

- An excellent biasing technique for discrete MOSFET circuits consists of fixing the dc voltage at the gate, V_G, and connecting a resistance in the source lead, as shown in Fig.4.30(a). For this circuit we

$$V_G = V_{GS} + R_S I_D \tag{4.46}$$

- Resistor R_s provides *negative feedback*, which acts to stabilize the value of the bias current I_D.
- R_s gives it the name **degeneration resistance**.

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- Figure 4.30(b) provides a graphical illustration of the effectiveness of this biasing scheme.
- The intersection of this straight line with the i_D-V_{GS} characteristic curve provides the coordinates (I_D and V_{GS}) of the bias point.
- Observe that compared to the case of fixed V_{GS}, here the variability obtained in I_D is much smaller.
- Two possible practical discrete implementations of this bias scheme are shown in Fig. 4.30(c) and (e).

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EXAMPLE 4.9

It is required to design the circuit of Fig. 4.30(c) to establish a dc drain current $I_D = 0.5$ mA. The MOSFET is specified to have $V_t = 1$ V and $k_n'W/L = 1$ mA/V^2. For simplicity, neglect the channel-length modulation effect (i.e., assume $\lambda = 0$). Use a power-supply $V_{DD} = 15$ V. Calculate the percentage change in the value of I_D obtained when the MOSFET is replaced with another unit having the same $k_n'W/L$ but $V_t = 1.5$ V.

Solution

As a rule of thumb for designing this classical biasing circuit, we choose R_D and R_S to provide one-third of the power-supply voltage V_{DD} as a drop across each of R_D, the transistor (i.e., V_{DS}) and R_S. For $V_{DD} = 15$ V, this choice makes $V_D = +10$ V and $V_S = +5$ V. Now, since I_D is required to be 0.5 mA, we can find the values of R_D and R_S as follows:

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{15 - 10}{0.5} = 10\ \text{k}\Omega$$

$$R_S = \frac{V_S}{R_S} = \frac{5}{0.5} = 10\ \text{k}\Omega$$

The required value of V_{GS} can be determined by first calculating the overdrive voltage V_{OV} from

$$I_D = \tfrac{1}{2}k_n'(W/L)V_{OV}^2$$

$$0.5 = \tfrac{1}{2} \times 1 \times V_{OV}^2$$

which yields $V_{OV} = 1$ V, and thus,

$$V_{GS} = V_t + V_{OV} = 1 + 1 = 2\ \text{V}$$

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Now, since $V_S = +5$ V, V_G must be

$$V_G = V_S + V_{GS} = 5 + 2 = 7 \text{ V}$$

To establish this voltage at the gate we may select $R_{G1} = 8$ MΩ and $R_{G2} = 7$ MΩ. The final circuit is shown in Fig. 4.31. Observe that the dc voltage at the drain (+10 V) allows for a positive signal swing of +5 V (i.e., up to V_{DD}) and a negative signal swing of –4 V [i.e., down to $(V_G - V_t)$].

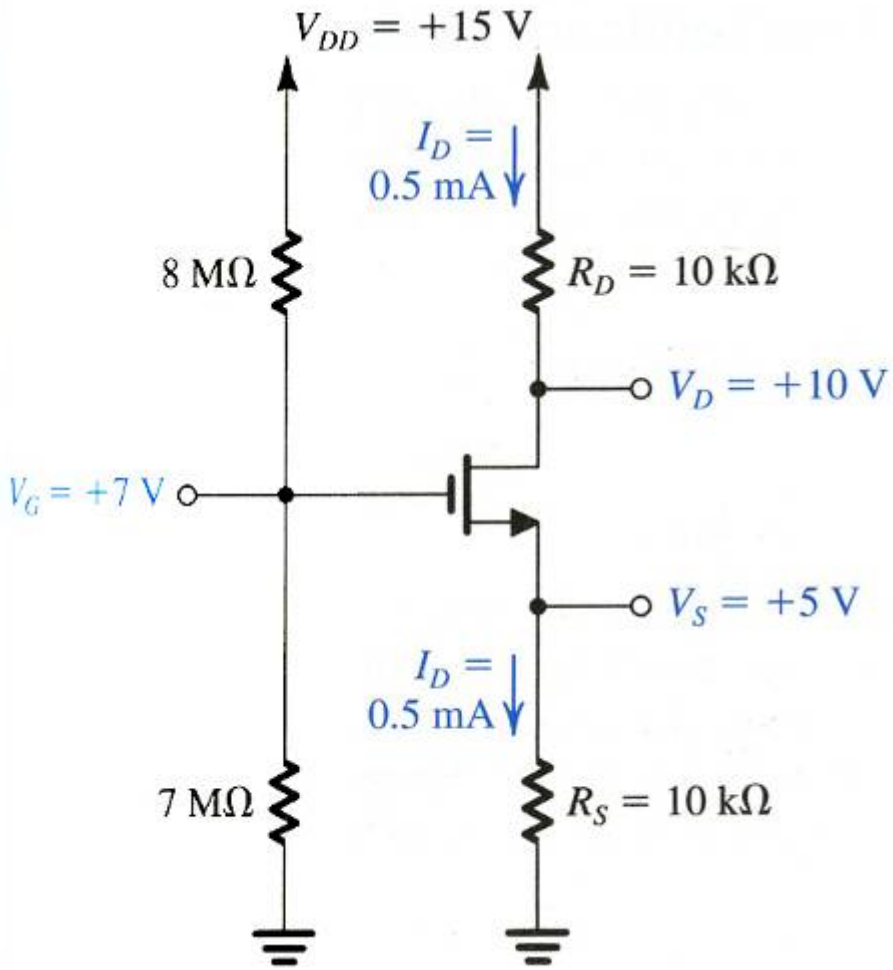

FIGURE 4.31 Circuit for Example 4.9.

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If the NMOS transistor is replaced with another having $V_t = 1.5$ V, the new value of I_D can be found as follows:

$$I_D = \tfrac{1}{2} \times 1 \times (V_{GS} - 1.5)^2 \tag{4.47}$$

$$V_G = V_{GS} + I_D R_S$$

$$7 = V_{GS} + 10 I_D \tag{4.48}$$

Solving Eqs. (4.47) and (4.48) together yields

$$I_D = 0.455 \text{ mA}$$

Thus the change in I_D is

$$\Delta I_D = 0.455 - 0.5 = -0.045 \text{ mA}$$

which is $\dfrac{-0.045}{0.5} \times 100 = -9\%$ change.

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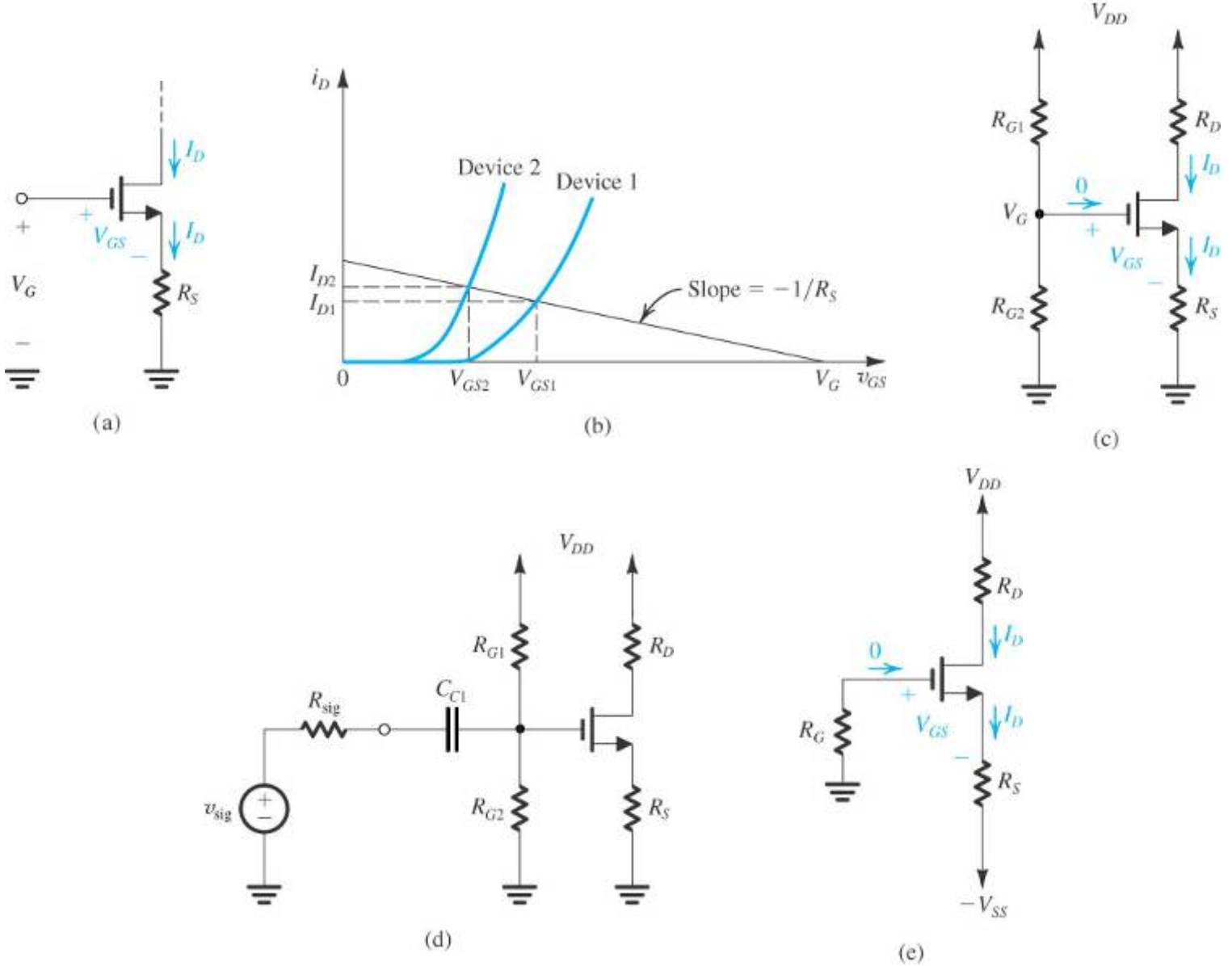

Figure 4.30 Biasing using a fixed voltage at the gate, V_G, and a resistance in the source lead, R_S: **(a)** basic arrangement; **(b)** reduced variability in I_D; **(c)** practical implementation using a single supply; **(d)** coupling of a signal source to the gate using a capacitor C_{C1}; **(e)** practical implementation using two supplies.

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4.5.3 Biasing Using a Drain-to-Gate Feedback Resistor

- Fig. 4.32. Here the large feedback resistance R_G (usually in the MΩ range) forces the dc voltage at the gate to be equal to that at the drain (because I_G=0). Thus we can write

$$V_{GS}=V_{DS}=V_{DD}-R_D I_D$$

$$V_{DD}=V_{GS}+R_D I_D \qquad (4.49)$$

which is identical in form to Eq. (4.46).

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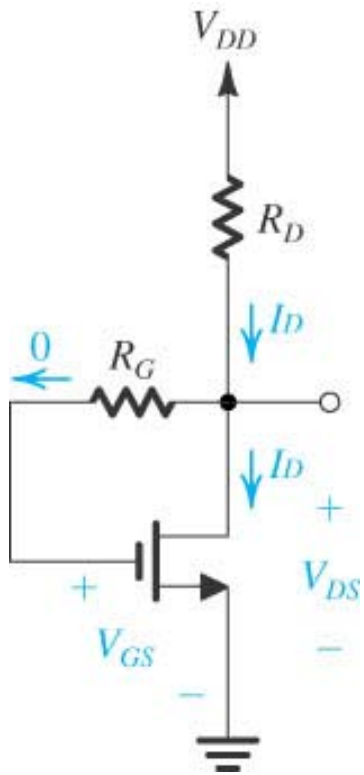

Figure 4.32 Biasing the MOSFET using a large drain-to-gate feedback resistance, R_G.

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4.5.4 Biasing Using a Constant-Current Source

- The most effective scheme for biasing a MOSFET amplifier is that using a constant-current source.
- Figure 4.33(a) shows such an arrangement applied to a discrete MOSFET.
- A circuit for implementing the constant-current source I is shown in Fig. 4.33(b).

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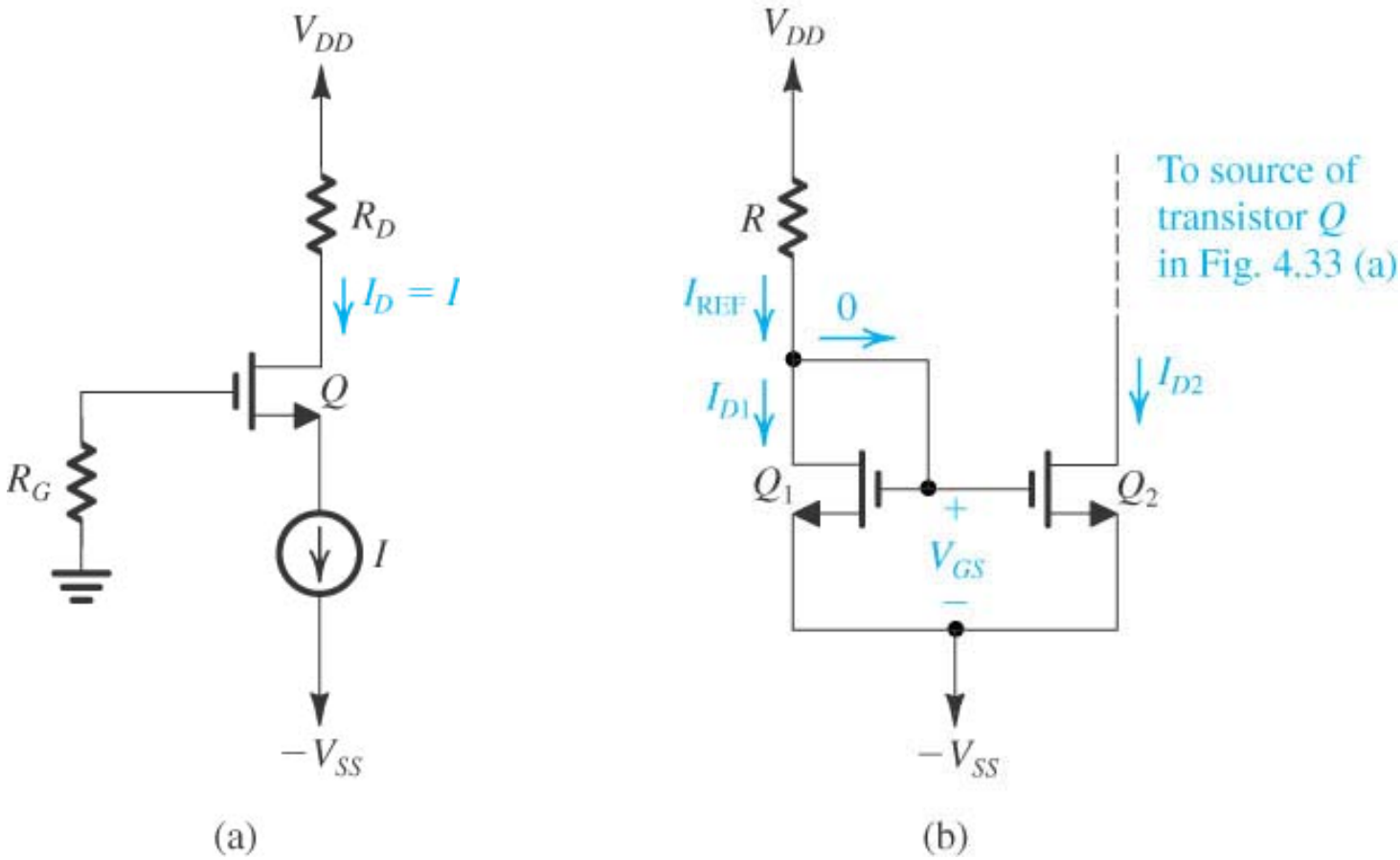

Figure 4.33 **(a)** Biasing the MOSFET using a constant-current source I. **(b)** Implementation of the constant-current source I using a current mirror.

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- Transistor Q_1,whose drain is shorted to its gate and thus is operating in the saturation region, such that

$$I_{D1} = \frac{1}{2} k'_n \left(\frac{W}{L}\right)_1 (V_{GS} - V_t)^2 \qquad (4.50)$$

where we have neglected channel-length modulation (i.e., assumed $\lambda=0$)

- The drain current of Q_1 is supplied by V_{DD} through resistor R. Since the gate currents are zero,

$$I_{D1} = I_{REF} = \frac{V_{DD} + V_{SS} - V_{GS}}{R} \qquad (4.51)$$

R is considered to be the *reference current* of the current source and is denoted I_{REF}.

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- Now consider transistor Q_2: It has the same V_{GS} as Q_1; thus if we assume that it is operating in saturation, its drain current, which is the desired current I of the current source, will be

$$I = I_{D2} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_2 (V_{GS} - V_t)^2 \qquad (4.52)$$

  where we have neglected channel-length modulation.
- Equation (4.51) and (4.52) enable us to relate the current I to the reference current I_{REF},

$$I = I_{REF} \frac{(W/L)_2}{(W/L)_1} \qquad (4.53)$$

- This circuit, known as a **current mirror**, is very popular in the design of IC MOS amplifiers.

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4.6 SMALL-SIGNAL OPERATION AND MODELS

- Section 4.4 we learned that linear amplification can be obtained by biasing the MOSFET to operate in the saturation region and by keeping the input signal small.

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4.6.1 The DC Bias Point

- The dc bias current I_D can be found by setting the signal v_{gs} to zero; thus,

$$I_D = \frac{1}{2} k'_n \frac{W}{L} (V_{GS} - V_t)^2 \qquad (4.54)$$

- The dc voltage at the drain, V_{DS} or simply V_D (since S is ground), will be

$$V_D = V_{DD} - R_D I_D \qquad (4.55)$$

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- To ensure saturation-region operation, we must have

$$V_D > V_{GS} - V_t$$

- Furthermore, since the total voltage at the drain will have a signal component superimposed on V_D , V_D has to be sufficiently greater than $(V_D - V_t)$ to allow for the required signal swing.

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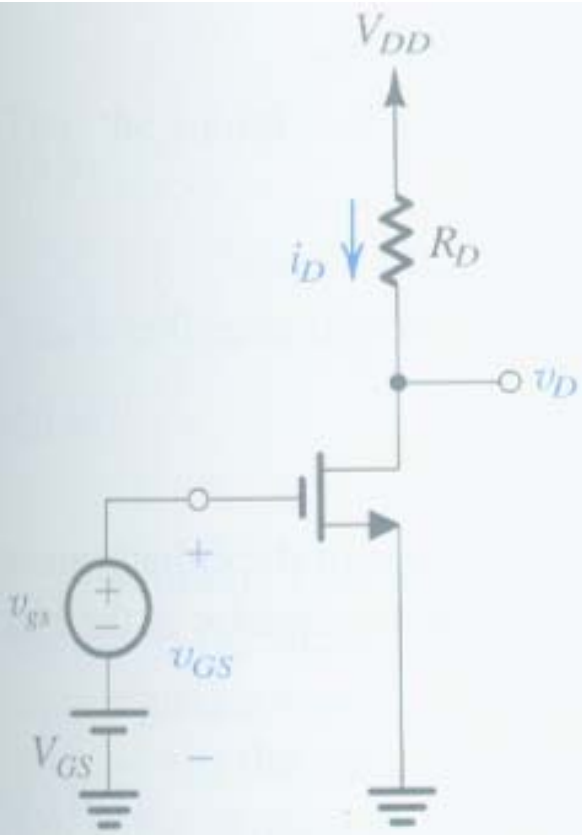

FIGURE 4.34 Conceptual circuit utilized to study the operation of the MOSFET as a small-signal amplifier.

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4.6.2 The Signal Current in the Drain Terminal

- Next, consider the situation with the input signal v_{gs} applied. The total instantaneous gate-to-source voltage will be

$$v_{GS} = V_{GS} + v_{gs} \tag{4.56}$$

- resulting in a total instantaneous drain current i_D ,

$$i_D = \frac{1}{2}k'_n \frac{W}{L}(V_{GS} + v_{gs} - V_t)^2$$

$$= \frac{1}{2}k'_n \frac{W}{L}(V_{GS} - V_t)^2 + k'_n \frac{W}{L}(V_{GS} - V_t)v_{gs} + \frac{1}{2}k'_n \frac{W}{L}v_{gs}^2 \tag{4.57}$$

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- The first term on the right-hand side of Eq.(4.57) can be recognized as the dc bias current I_D (Eq. 4.54). The third term represents a current component that is proportional to the input signal v_{gs} .The third term is a current component that is proportional to the square of the input signal.

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- To reduce the nonlinear distortion introduced by the MOSFET, the input signal should be kept small so that

$$\frac{1}{2}k'_n\frac{W}{L}v_{gs}^2 \ll k'_n\frac{W}{L}(V_{GS}-V_t)v_{gs}$$

- Resulting in

$$v_{gs} \ll 2(V_{GS}-V_t) \qquad (4.58)$$

- Or, equivalently,

$$v_{gs} \ll 2V_{OV} \qquad (4.59)$$

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- If this **small-signal condition** is satisfied, we may neglect the last term in Eq. (4.57) and express i_D as

$$i_D \simeq I_D + i_d$$

- Where

$$i_d = k'_n \frac{W}{L}(V_{GS} - V_t)v_{gs}$$

- The parameter that relates i_d and v_{gs} is the MOSFET **transconductance** g_m ,

$$g_m \equiv \frac{i_d}{v_{gs}} = k'_n \frac{W}{L}(V_{GS} - V_t)$$

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- Figure 4.35 presents a graphical interpretation of the small-signal operation of the enhancement MOSFET amplifier.

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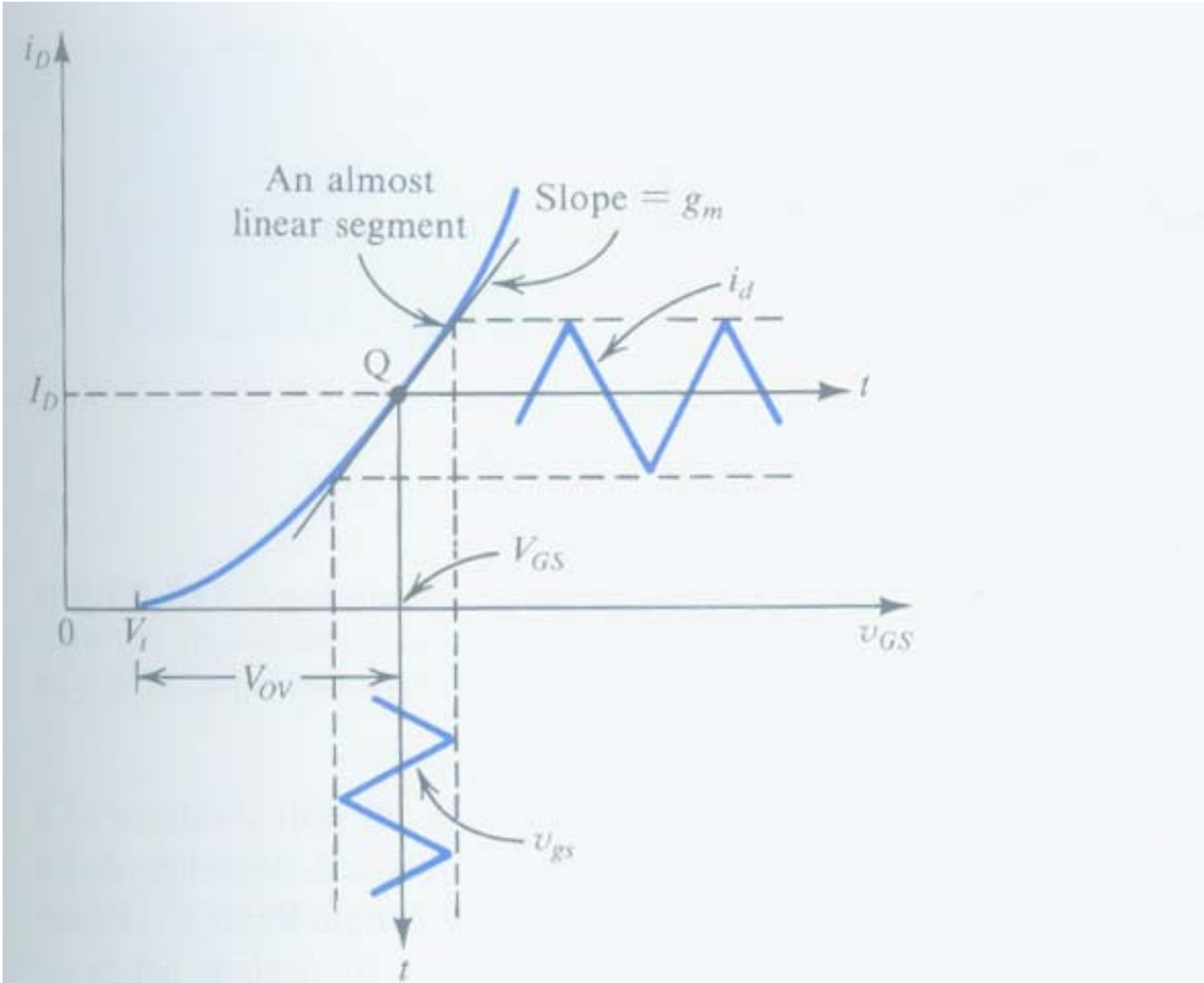

FIGURE 4.35 Small-signal operation of the enhancement MOSFET amplifier.

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4.6.3 The Voltage Gain

- Returning to the circuit of Fig. 4.34, we can express the total instantaneous drain voltage v_D as follows:

$$v_D = V_{DD} - R_D i_D$$

$$v_D = V_{DD} - R_D (I_D + i_d)$$

$$v_D = V_D - R_D i_d - R_D I_D$$

- The signal component

$$v_d = -i_d R_D = -g_m v_{gs} R_D \qquad (4.64)$$

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- Voltage gain is given by

$$A_v \equiv \frac{v_d}{v_{gs}} = -g_m R_D \qquad (4.65)$$

- This is illustrated in Fig. 4.36, which shows v_{GS} and v_D.

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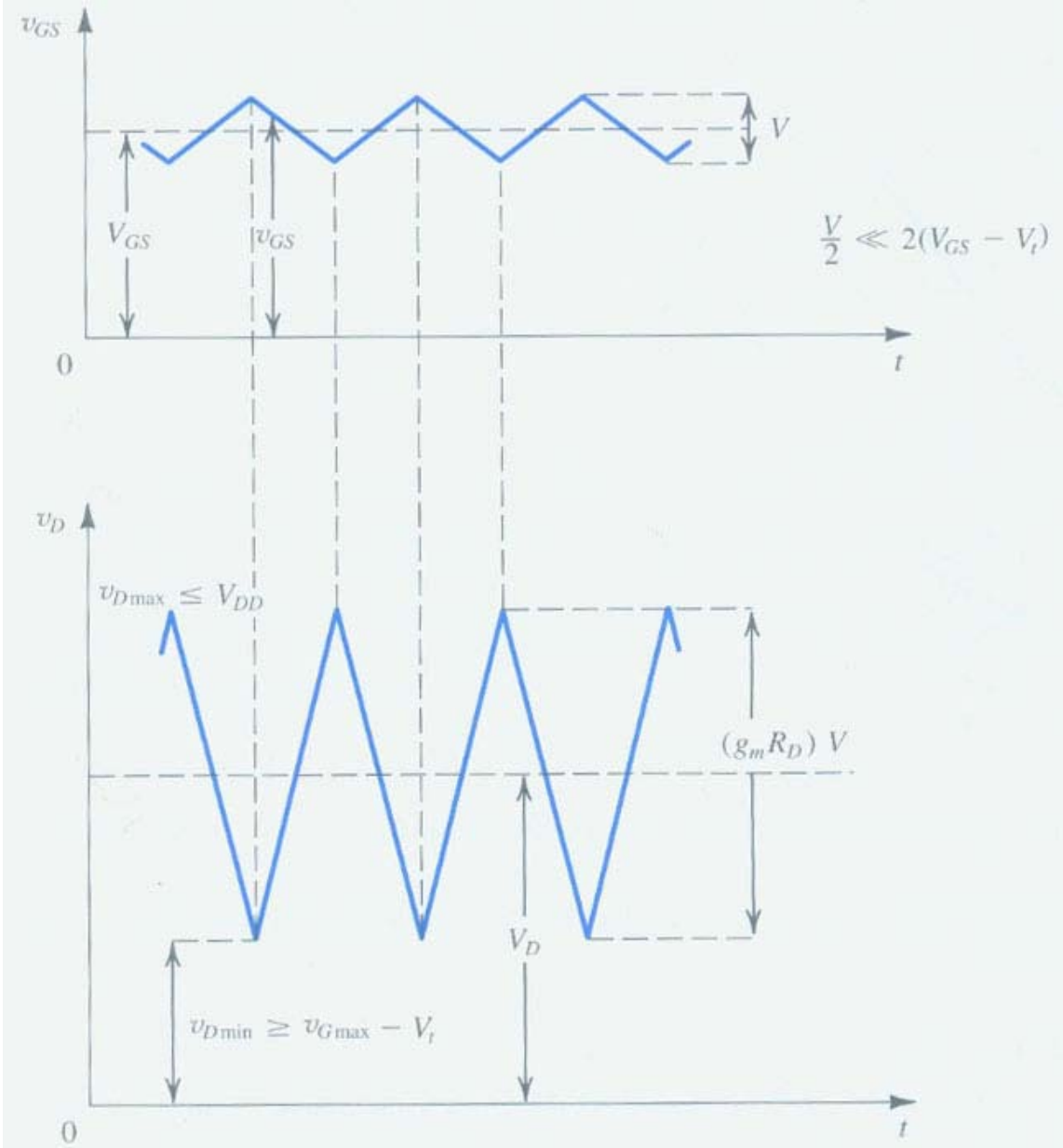

FIGURE 4.36 Total instantaneous voltages v_{GS} and v_D for the circuit in Fig. 4.34.

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4.7 SINGLE-STAGE MOS AMPLIFIERS

4.7.1 The Basic Structure

- Figure 4.42 shows the basic circuit we shall utilize to implement the various configurations of discrete-circuit MOS amplifiers.

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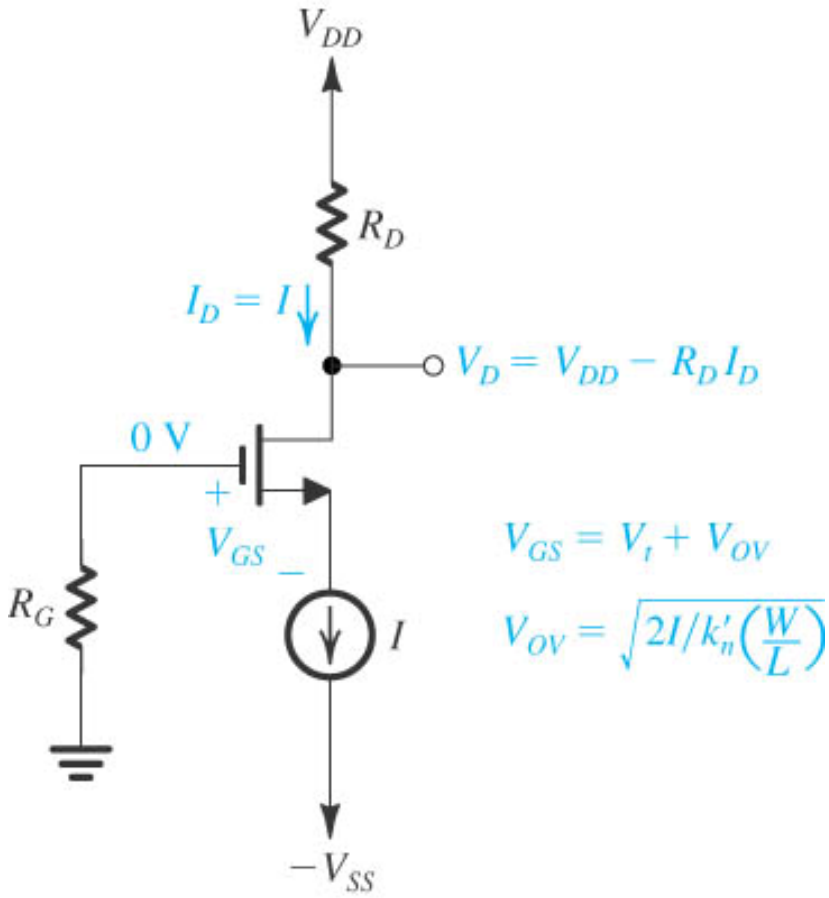

Figure 4.42 Basic structure of the circuit used to realize single-stage discrete-circuit MOS amplifier configurations.

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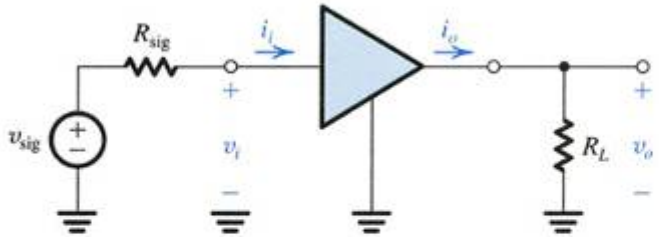
TABLE 4.3 Characteristic Parameters of Amplifiers

Circuit



Definitions

- Input resistance with no load:

$$R_i \equiv \left.\frac{v_i}{i_i}\right|_{R_L=\infty}$$

- Input resistance:

$$R_{in} \equiv \frac{v_i}{i_i}$$

- Open-circuit voltage gain:

$$A_{vo} \equiv \left.\frac{v_o}{v_i}\right|_{R_L=\infty}$$

- Voltage gain:

$$A_v \equiv \frac{v_o}{v_i}$$

- Short-circuit current gain:

$$A_{is} \equiv \left.\frac{i_o}{i_i}\right|_{R_L=0}$$

- Current gain:

$$A_i \equiv \frac{i_o}{i_i}$$

- Short-circuit transconductance:

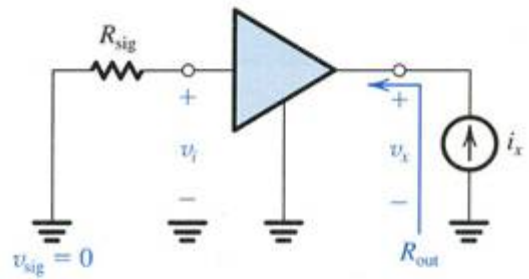
$$G_m \equiv \left.\frac{i_o}{v_i}\right|_{R_L=0}$$

- Output resistance of amplifier proper:

$$R_o \equiv \left.\frac{v_x}{i_x}\right|_{v_i=0}$$

- Output resistance:

$$R_{out} \equiv \left.\frac{v_x}{i_x}\right|_{v_{sig}=0}$$

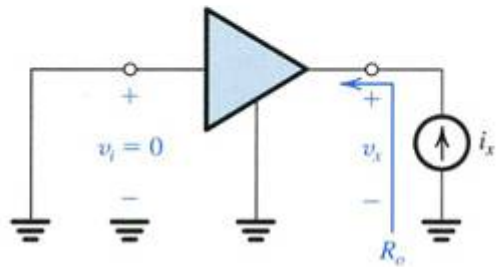


- Open-circuit overall voltage gain:

$$G_{vo} \equiv \left.\frac{v_o}{v_{sig}}\right|_{R_L=\infty}$$

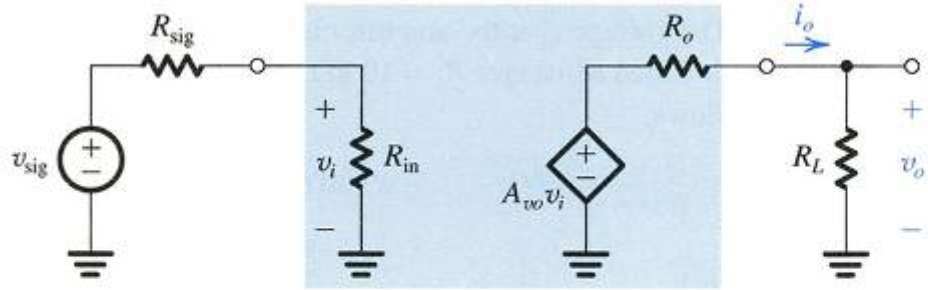
- Overall voltage gain:

$$G_v \equiv \frac{v_o}{v_{sig}}$$

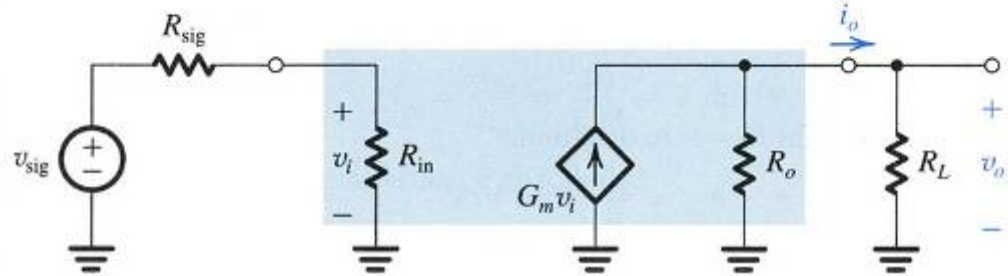


Equivalent Circuits

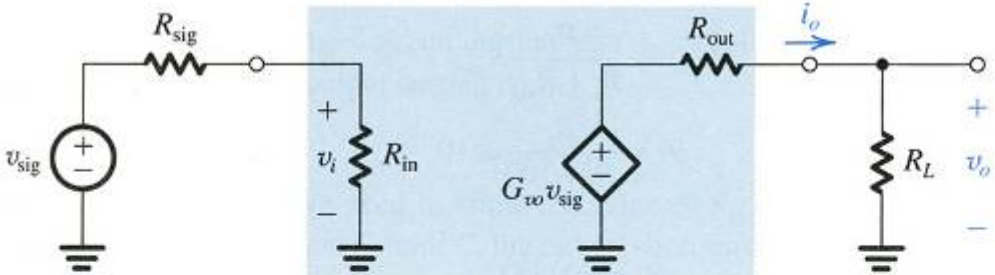
- A:



- B:



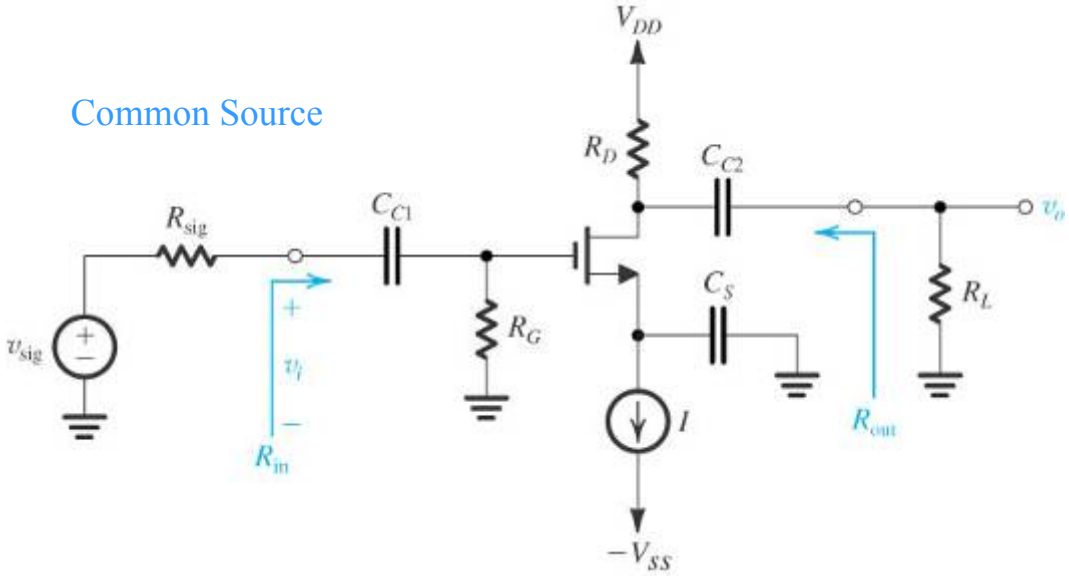
- C:



Relationships

- $\dfrac{v_i}{v_{sig}} = \dfrac{R_{in}}{R_{in} + R_{sig}}$
- $A_v = A_{vo}\dfrac{R_L}{R_L + R_o}$
- $A_{vo} = G_m R_o$
- $G_v = \dfrac{R_{in}}{R_{in} + R_{sig}} A_{vo} \dfrac{R_L}{R_L + R_o}$
- $G_{vo} = \dfrac{R_i}{R_i + R_{sig}} A_{vo}$
- $G_v = G_{vo}\dfrac{R_L}{R_L + R_{out}}$

Common Source



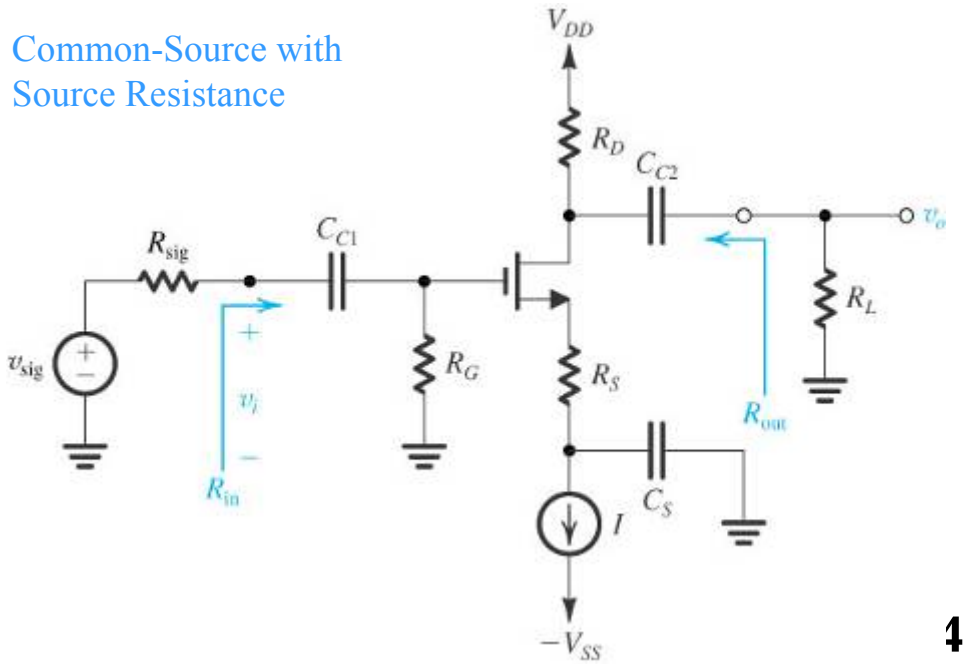
$$R_{in} = R_G$$

$$A_v = -g_m(r_O \parallel R_D \parallel R_L)$$

$$Rout = rO \parallel RD$$

$$G_v = -\frac{R_G}{R_G + R_{sig}} g_m(r_O \parallel R_D \parallel R_L)$$

Common-Source with Source Resistance



Neglecting r_O :

$$R_{in} = R_G$$

$$A_v = -\frac{R_D \parallel R_L}{\frac{1}{g_m} + R_S} = -\frac{g_m(R_D \parallel R_L)}{1 + g_m R_S}$$

$$Rout = RD$$

$$G_v = -\frac{R_G}{R_G + R_{sig}} \frac{g_m(R_D \parallel R_L)}{1 + g_m R_S}$$

$$\frac{v_{gs}}{v_i} = \frac{1}{1 + g_m R_S}$$

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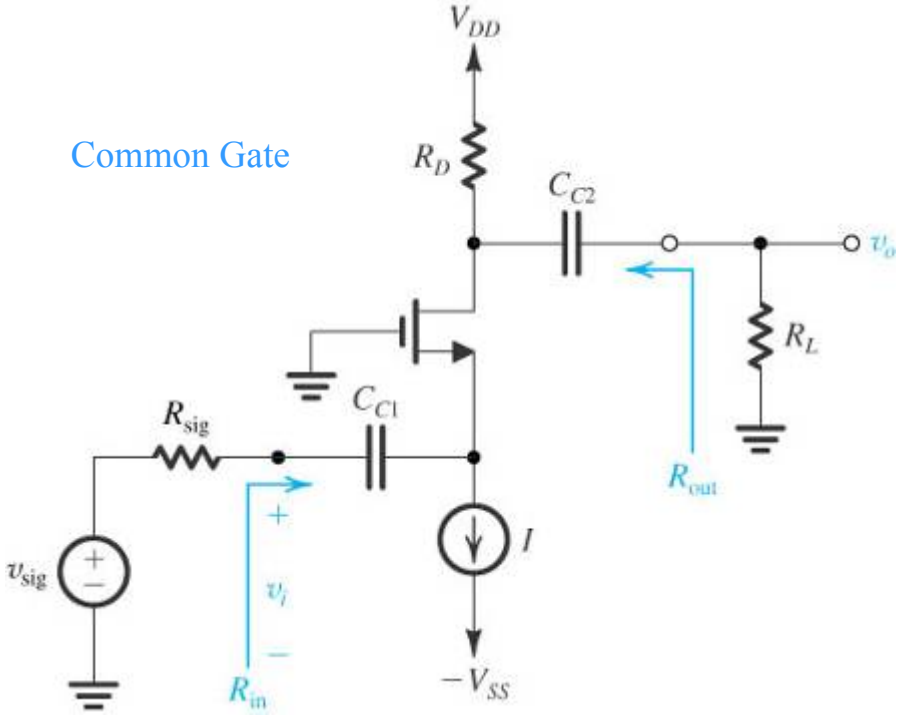
Common Gate



Neglecting r_O :

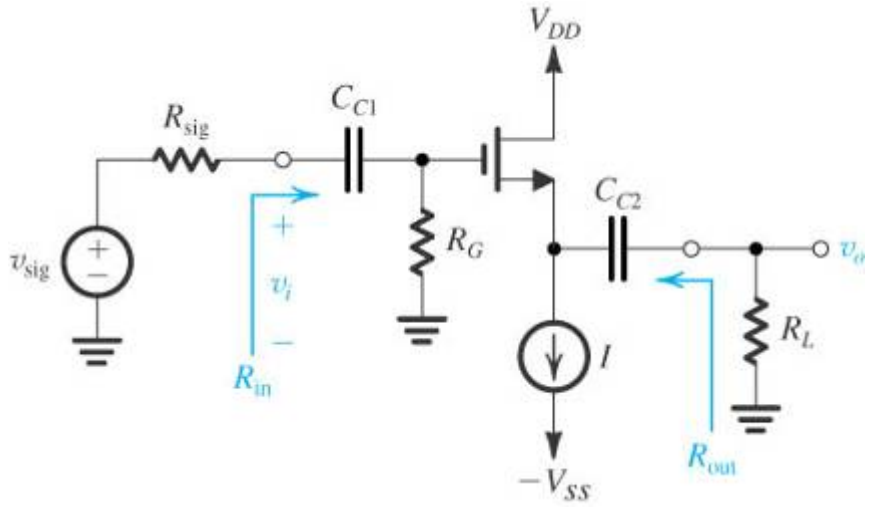
$$R_{in} = \frac{1}{g_m}$$

$$A_v = g_m(R_D \parallel R_L)$$

$$R_{out} = R_D$$

$$G_v = \frac{1}{1+g_m R_{sig}} g_m(R_D \parallel R_L)$$

Common-Drain or Source Follower



$$R_{in} = R_G$$

$$A_v = \frac{r_O \parallel R_L}{(r_O \parallel R_L) + \dfrac{1}{g_m}}$$

$$R_{out} = r_O \parallel g_m \cong \frac{1}{g_m}$$

$$G_v = \frac{R_G}{R_G + R_{sig}} \frac{r_O \parallel R_L}{(r_O \parallel R_L) + \dfrac{1}{g_m}}$$

Table 4.4 *(Continued)*

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4.10 THE CMOS DIGITAL LOGIC INVERTER

- For any IC technology used in digital circuit design, the basic circuit element is the logic inverter.
- Once the operation and characteristics of the inverter circuit are thoroughly understood, the results can be extended to the design of logic gates and other more complex circuits.
- The basic CMOS inverter is shown in Fig. 4.53.It utilizes two matched enhancement-type MOSFETs: one, Q_N, with an n channel and the other, Q_P, with a p channel.

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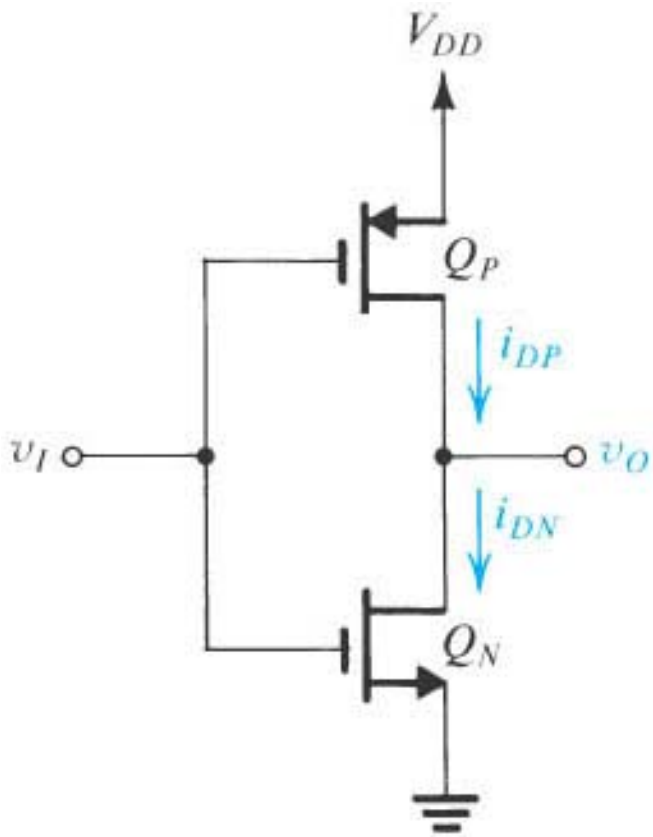

Figure 4.53 The CMOS inverter.

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4.10.1 Circuit Operation

- Two extreme cases: when v_I is at logic-0 level, which is approximately 0V; is at logic-0 level, which is approximately 0V; and when v_I is at logic-1 level, which is approximately V_{DD}V.
- Figure 4.54 illustrates the case when $v_I=V_{DD}$, showing the i_D-v_{DS} characheristic curve for Q_N with $v_{GSN}=V_{DD}$ (note that $i_D=I$ and $v_{DSN}=v_O$). Superimposed on the Q_N characteristic curve is the load curve, which is the i_D-v_{DS} curve of for the case $v_{SGP}=0$.

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- Since $v_{SGP}<|V_t|$, the load curve will be a horizontal straight line at almost zero current level. The operation point will be at the intersection of the two curves.
- Although Q_N is operating at nearly zero current, the operating point is on a steep segment of the i_D-v_{DS} curve. Thus Q_N provides a low-resistance path between the output terminal and ground with (triode region):

$$r_{DSN} = 1/[k_n'\left(\frac{W}{L}\right)_n (V_{DD} - V_{tn})]$$

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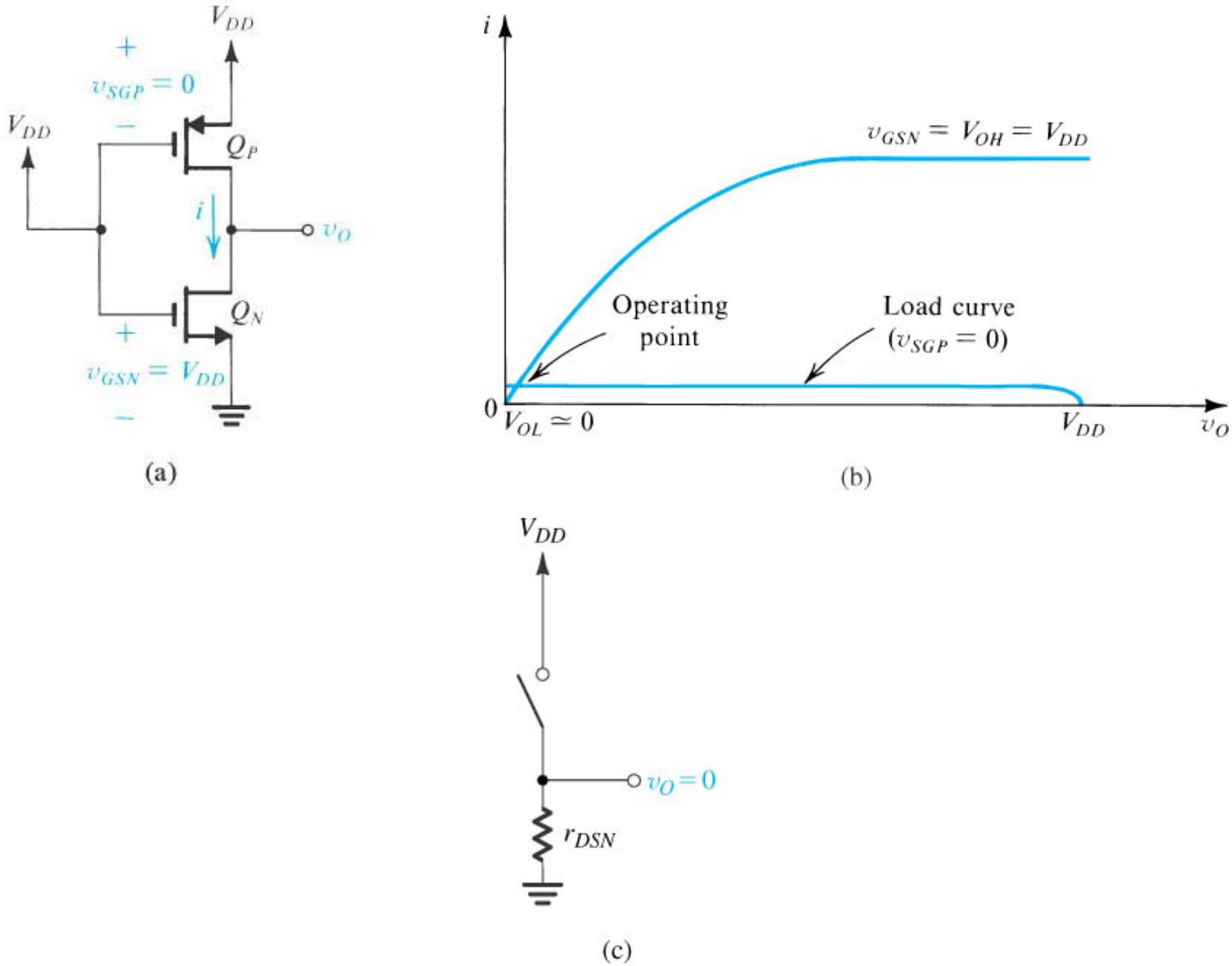

Figure 4.54 Operation of the CMOS inverter when v_I is high: **(a)** circuit with $v_I = V_{DD}$ (logic-1 level, or V_{OH}); **(b)** graphical construction to determine the operating point; **(c)** equivalent circuit.

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- Similarly, when v_I=0V, Q_P provides a low-resistance path between the output terminal and the dc supply with (triode region):

$$r_{DSP} = 1/[k_p^{'}\left(\frac{W}{L}\right)_p (V_{DD} - V_{tp})]$$

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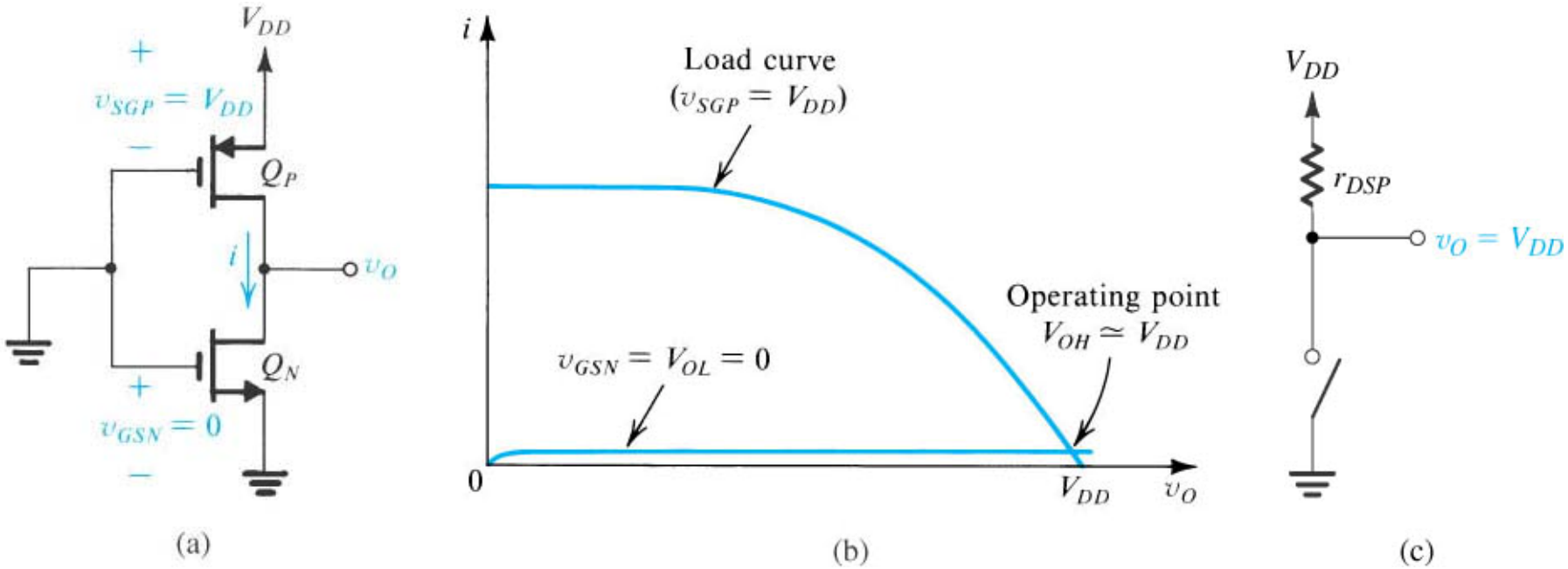

Figure 4.55 Operation of the CMOS inverter when v_I is low: **(a)** circuit with $v_I = 0$ V (logic-0 level, or V_{OL}); **(b)** graphical construction to determine the operating point; **(c)** equivalent circuit.

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4.10.2 The Voltage Transfer Characteristic

- For Q_N

$$i_{DN} = k_n'\left(\frac{W}{L}\right)_n[(v_I - V_{tn})v_O - \frac{1}{2}v_O^2], \text{ for } v_O \le v_I - V_{tn}$$

$$i_{DN} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_n(v_I - V_{tn})^2, \text{ for } v_O \ge v_I - V_{tn}$$

- For Q_P

$$i_{DP} = k_p'\left(\frac{W}{L}\right)_p[(V_{DD} - v_I - |V_{tp}|)(V_{DD} - v_O) - \frac{1}{2}(V_{DD} - v_O)^2],$$

$$\text{for } v_O \ge v_I + |V_{tn}|$$

$$i_{DP} = \frac{1}{2}k_p'\left(\frac{W}{L}\right)_p(V_{DD} - v_I - |V_{tp}|)^2, \text{ for } v_O \le v_I + |V_{tp}|$$

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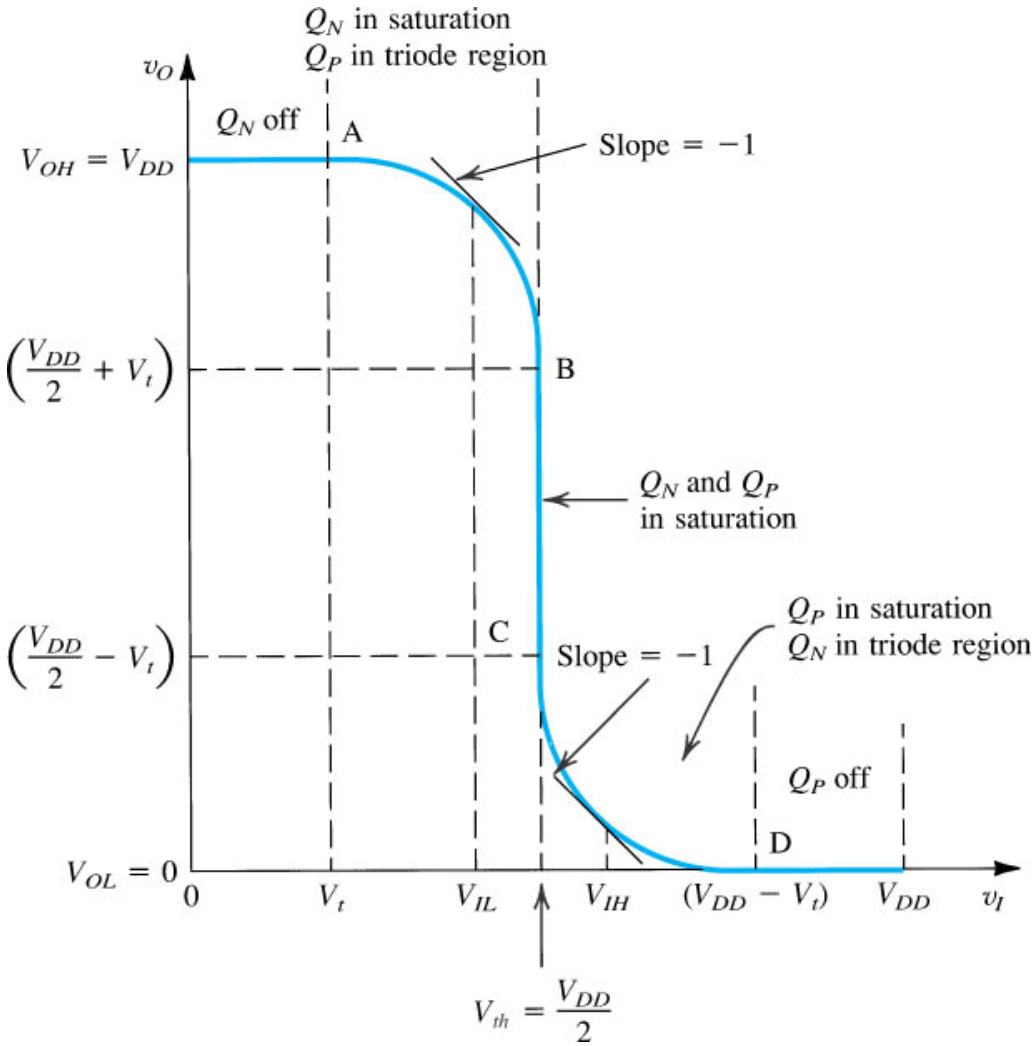

Figure 4.56 The voltage transfer characteristic of the CMOS inverter.

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- Figure 4.56 indicates the transfer characteristic has five distinct segment corresponding to different combinations of modes of operations on Q_N and Q_P.
- Segment BC is obtained when both MOSFETs are operating in the saturation region and is bounded by $v_O(B)=V_{DD}/2+V_t$, and $v_O(C)=V_{DD}/2-V_t$

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- Noise margin: the maximum permitted logic-0 or “low” level at the input V_{IL}, and the minimum permitted logic-1 or “high” level at the input V_{IH}.
- These are formally defined as the two points on the transfer curve at which the incremental gain is unity (i.e., the slope is -1)

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- To determine V_{IH}, we note that Q_N is in the triode region, and Q_P is in the saturation, and their corresponding currents are equal:

$$(v_I - V_t)v_O - \frac{1}{2}v_O^2 = \frac{1}{2}(V_{DD} - v_I - V_t)^2$$

$$\therefore (v_I - V_t)\frac{dv_O}{dv_I} + v_O - v_O\frac{dv_O}{dv_I} = -(V_{DD} - v_I - V_t)$$

substitute $v_I = V_{IH}$ and $dv_O / dv_I = -1$, we obtain

$v_O = V_{IH} - V_{DD}/2$, substitute this result to the first equation

we can obtain $V_{IH} = \frac{1}{8}(5V_{DD} - 2V_t)$

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- Use the symmetry relationship:

$$V_{IH} - \frac{1}{2}V_{DD} = \frac{1}{2}V_{DD} - V_{IL}$$

$$V_{IL} = \frac{1}{8}(3V_{DD} + 2V_t)$$

The noise margins can be determined as follows:

$$NM_H = V_{OH} - V_{IH} = V_{DD} - \frac{1}{8}(5V_{DD} - 2V_t)$$

$$= \frac{1}{8}(3V_{DD} + 2V_t)$$

$$NM_L = V_{IH} - V_{OH} = \frac{1}{8}(3V_{DD} + 2V_t) - 0$$

$$= \frac{1}{8}(3V_{DD} + 2V_t)$$

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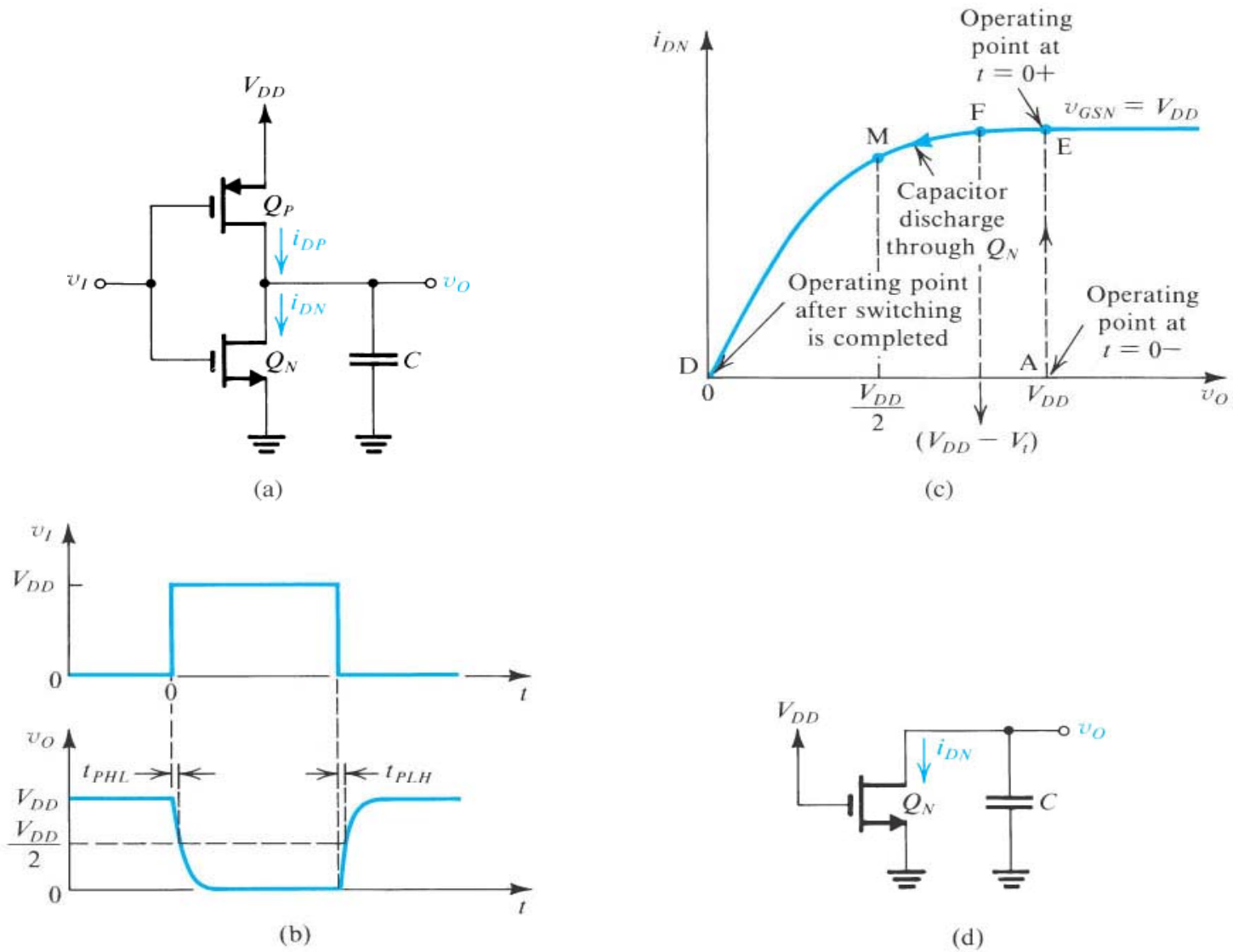

Figure 4.57 Dynamic operation of a capacitively loaded CMOS inverter: **(a)** circuit; **(b)** input and output waveforms; **(c)** trajectory of the operating point as the input goes high and C discharges through Q_N; **(d)** equivalent circuit during the capacitor discharge.

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